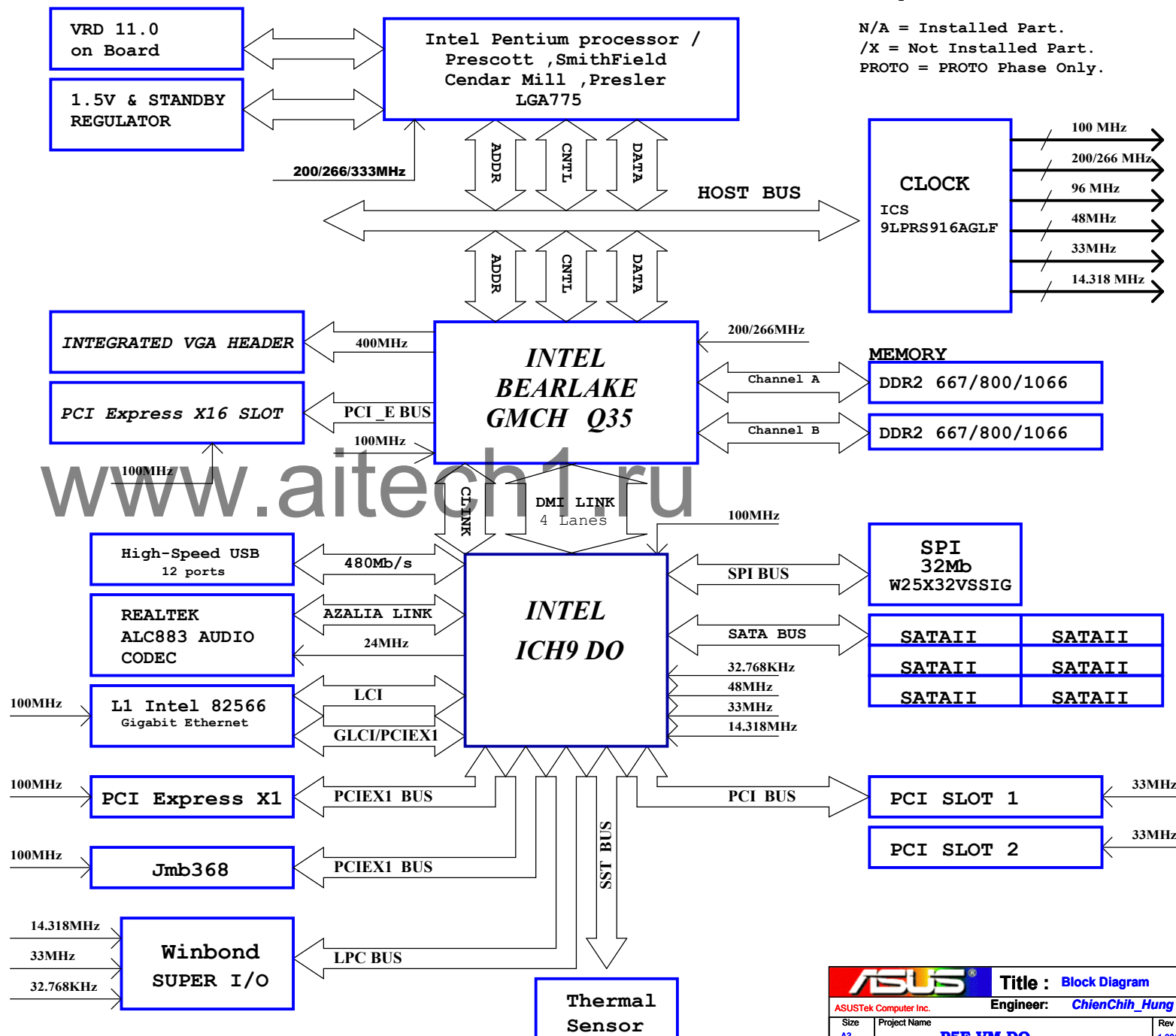


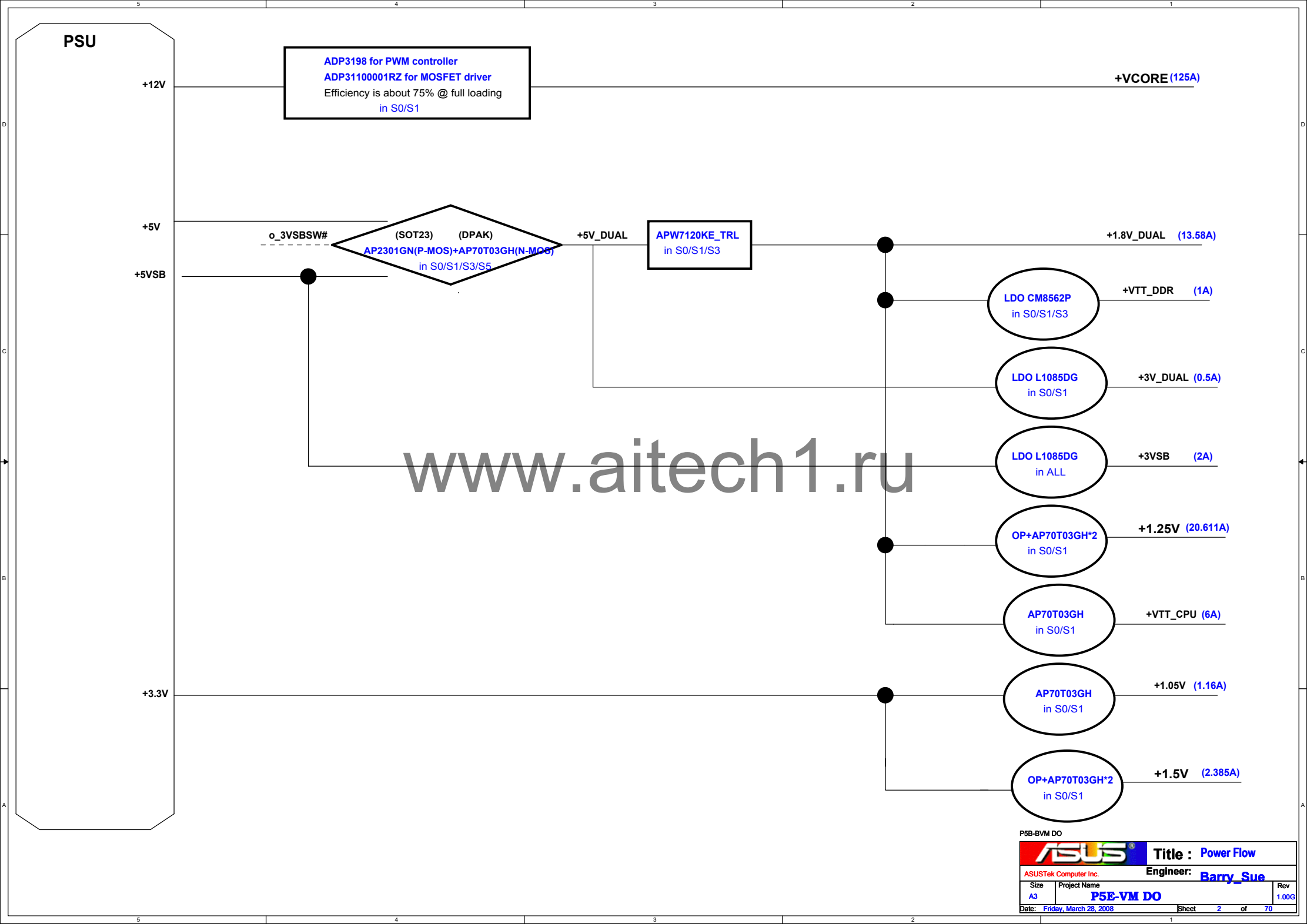
2007.08.24

CAD Note:
Default component footprint is
SMD 0402 type. Difference
footprint show on schematics.

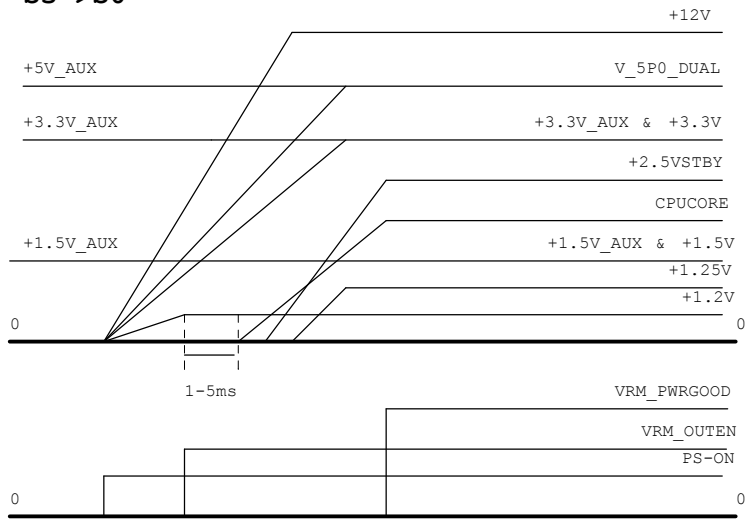
N/A = Installed Part.
/X = Not Installed Part.
PROTO = PROTO Phase Only.

PAGE	TITLE
01	BLOCK DIAGRAM
02	POWER FLOW CHART
03	POWER SEQUENCE
04	POWER DISTRIBUTION
05	CLOCK DISTRIBUTION
06	RESET MAP
07~08	Main clock
09~13	INTEL PROCESSOR LGA775
14~20	INTEL BEARLAKE
21	DDR2 CHANNEL A
22	DDR2 CHANNEL B
23	DDR2 POWER
24	Onboard VGA (BL)
25	LAN & USB Connector
26	PCIEX16 1
27	PCIEX1
28	PCI Slot
29	L1 Intel 82566 LAN
30	on board TPM
31~36	INTEL ICH9
37~38	AgereFW322
39	SATA Connector
40	JMB368
41	Audio ALC883 888
42	AUDIO CONNECTOR
43~48	USB Power circuit
49	TPM CONNECTOR
50	SPI
51~57	W83627DHG
58	POWER CONNECTOR
59	PANEL & HotStart
60	VCORE CONTROLLOR
61	VCORE DRIVERS
62	+5V DUAL& +3VSB&+3V DUAL
63	+1.5V
64	+1.8V DUAL& VTT DDR
65	+1.25VDUAL & +1.05V &+VTTCPU
66	+1.25V
67	NOS(Intel)
68	Screw Hole
69	EMI
70	Change PCB version List



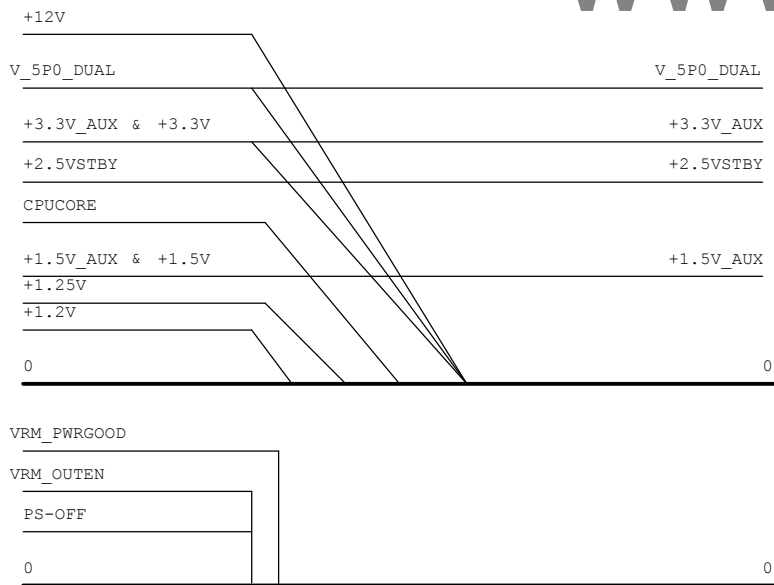


S5->S0

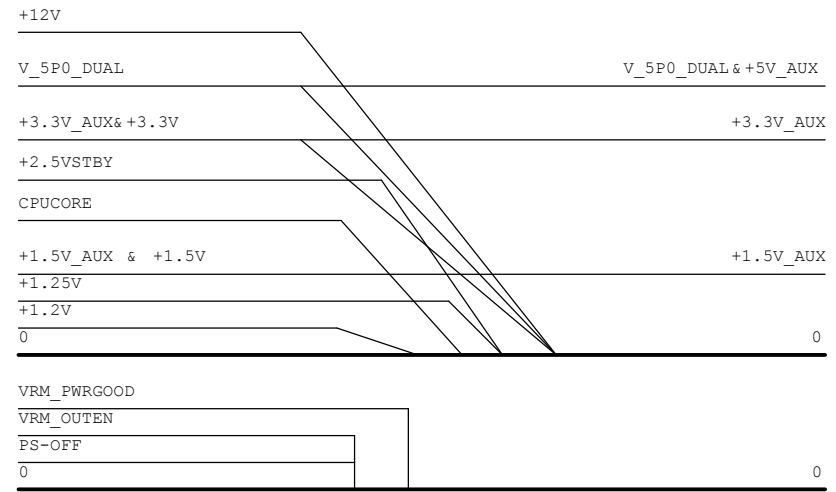


- 1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
- 2.VRM_OUTEN rises after the voltage across 90% of its specified value

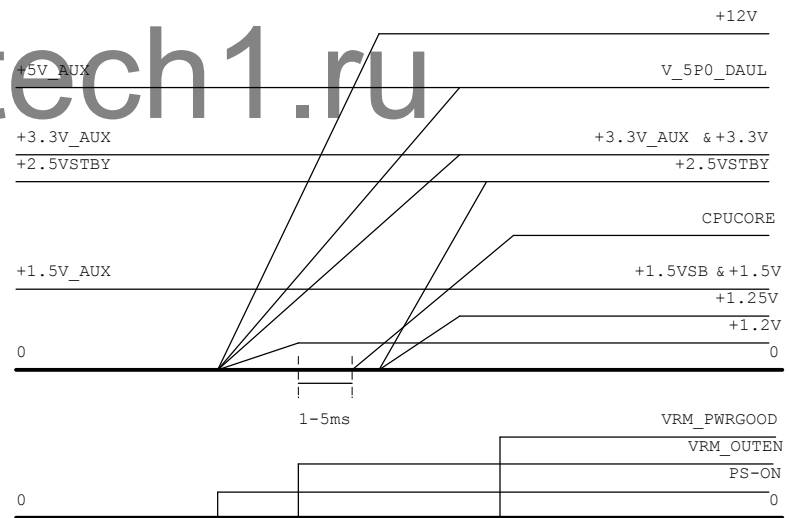
S0->S3



S0->S5



S3->S0



- 1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
- 2.VRM_OUTEN rises after the voltage across 90% of its specified value

- S0:** Windows Running+12V,V_5P0_DUAL,+3.3V,+3.3V_AUX,+2.5VSTBY,CPUCORE,+1.5V,+1.5V_AUX,+1.25V,+1.2V existed
S3: Windows StandbyV_5P0_DUAL,+3.3V_AUX,+1.5V_AUX,+2.5VSTBY existed
S5: AC Power On Only +5V_AUX,+3.3V_AUX,+1.5V_AUX existed

<Variant Name>

ASUS		Title : Power Sequence	
ASUSTek Computer Inc.		Engineer: Tyler_Yuan	
Size A3	Project Name P5E-VM DO		Rev 1.01G
Date: Friday, March 28, 2008		Sheet 3 of 70	

Prescott,Smithdield, Presler & Conroe	
VCORE	1.25A 130W
+1.2V_FSB_VTT	5.3A 6.36W

+1.8VSB	80mA	CK505
+3VSB	250mA	

Bear lake	
+1.5_DUAL	3.33A (S0,S1)
+1.5_DUAL	350mA (S3&SMCLK)
+1.2V_FSB	VTT 1.2A
+1.25V	13.8A
	2.47A (DMI&PCIE)
	4.9A (CL)
+3V	66mA (DAC)
	15.8mA (CMOS)

ICH9	
+1.2V_FSB_VTT	2mA
+1.5V	1.652A (USB&SATA&PLL)
	646mA (PCIE)
	15mA 0.0225W (CL internal)
	74mA 0.111W (LAN)
+1.25V	41mA (DMI)
+1.05V	1.43A (Core)
	37mA (CL internal)
	157mA 0.165W (10/100 LAN internal)
+3VSB	19mA (CL)
	32mA (HDA S3,S4&S5)
+3V	1mA (GbE-LAN)
	19mA (10/100 LAN)
	32mA (HDA S0&S1)
VCCRTC	308mA (VCC3_3)
	6uA

DDR2	
+1.8_DUAL	1.8A (S0,S1)
+1.8_DUAL	TBD (S3)
VTT_DDR	0.83A (S0)
	TBD (S3)

PCI EXPRESSx16	
+12V	5.5A 66W
+3VSB	0.375A 1.24W (wake)
+3VSB	20mA 66mW (no wake)
+3V	3.0A 9.9W

PCI SLOT	
+3VSB	0.375A 1.24W (wake)
+3VSB	20mA 66mW (no wake)
+3V	7.6A 25.08W
+5V	5A 25W
+12V	0.5A 6W
-12V	0.1A 1.2W

KB/MS	
+BUSB	0.5A 2.5W

USB 12 PORT	
BUSB+5V	2A (S0,S1)
BUSB+5V	15mA 75mW (S3)
FUSB+5V	4A (S0,S1)
FUSB+5V	10mA 50mW (S3)

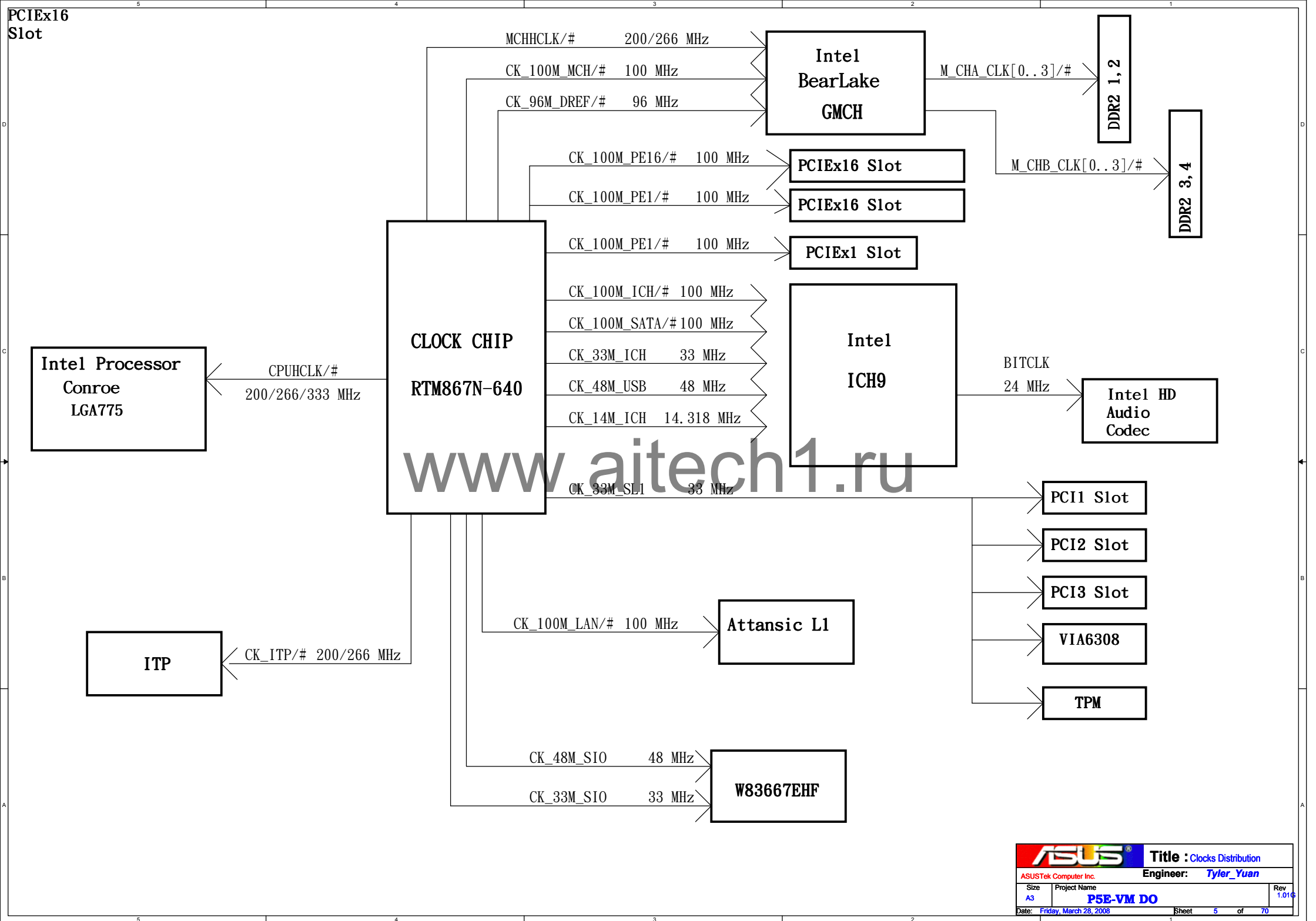
SPI	
+3VSB	30mA 99mW

FAN	
+12V	0.5A 6W

ALC885 CODEC	
+5VA	200mA 1W
+3V	40mA 132mW

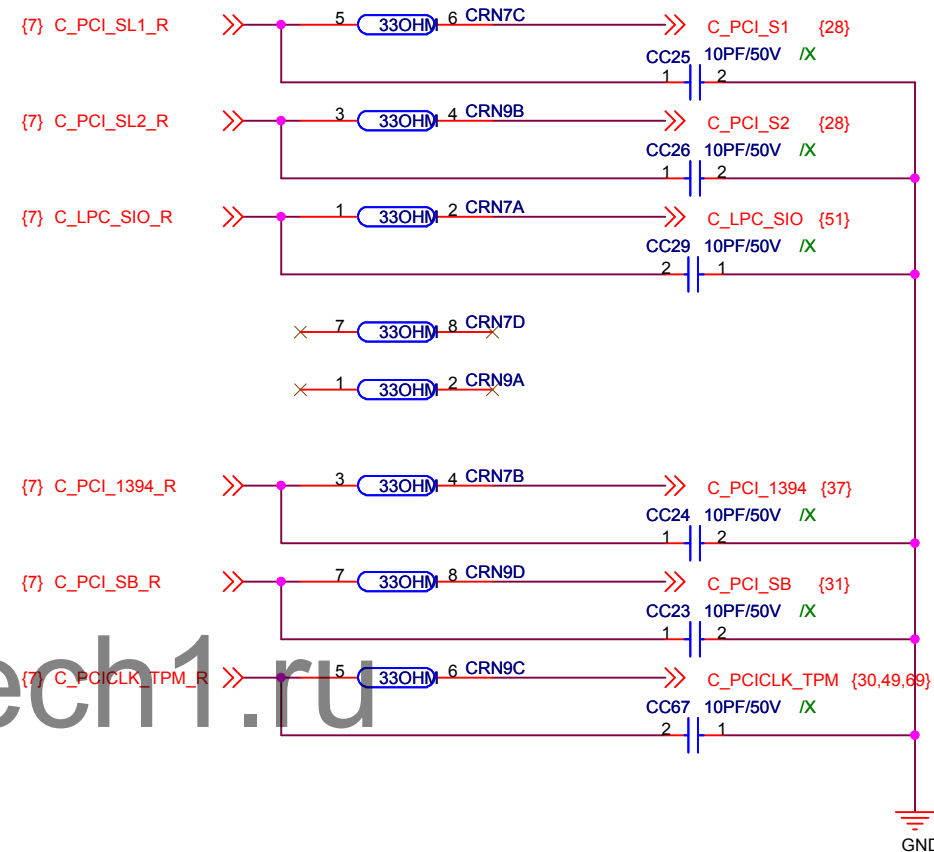
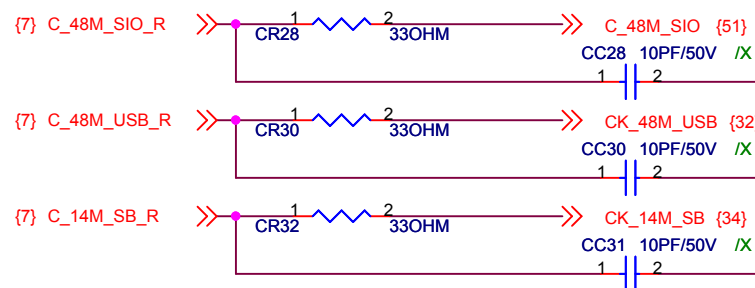
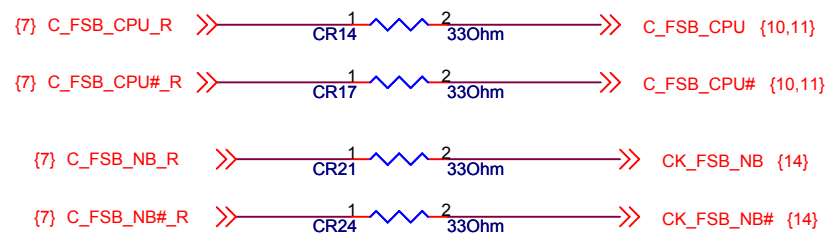
Atheros	
+3VSB	15.5mA 51.15mW (I/O&LED)
+2.5VSB	418.2mA 7.53W (Analog)
+1.5VSB	277.2mA 277.2mW (Core)

PCIEX1	
+12V	5.5A 66W
+3VSB	0.375A 1.24W (wake)
+3VSB	20mA 66mW (no wake)
+3V	3.0A 9.9W



- VCCSUS drives high when PWR CONN plug in.
- RSMRST# drives high from SIO to ICH9.
- SUSCLK sent out CLK from ICH9.

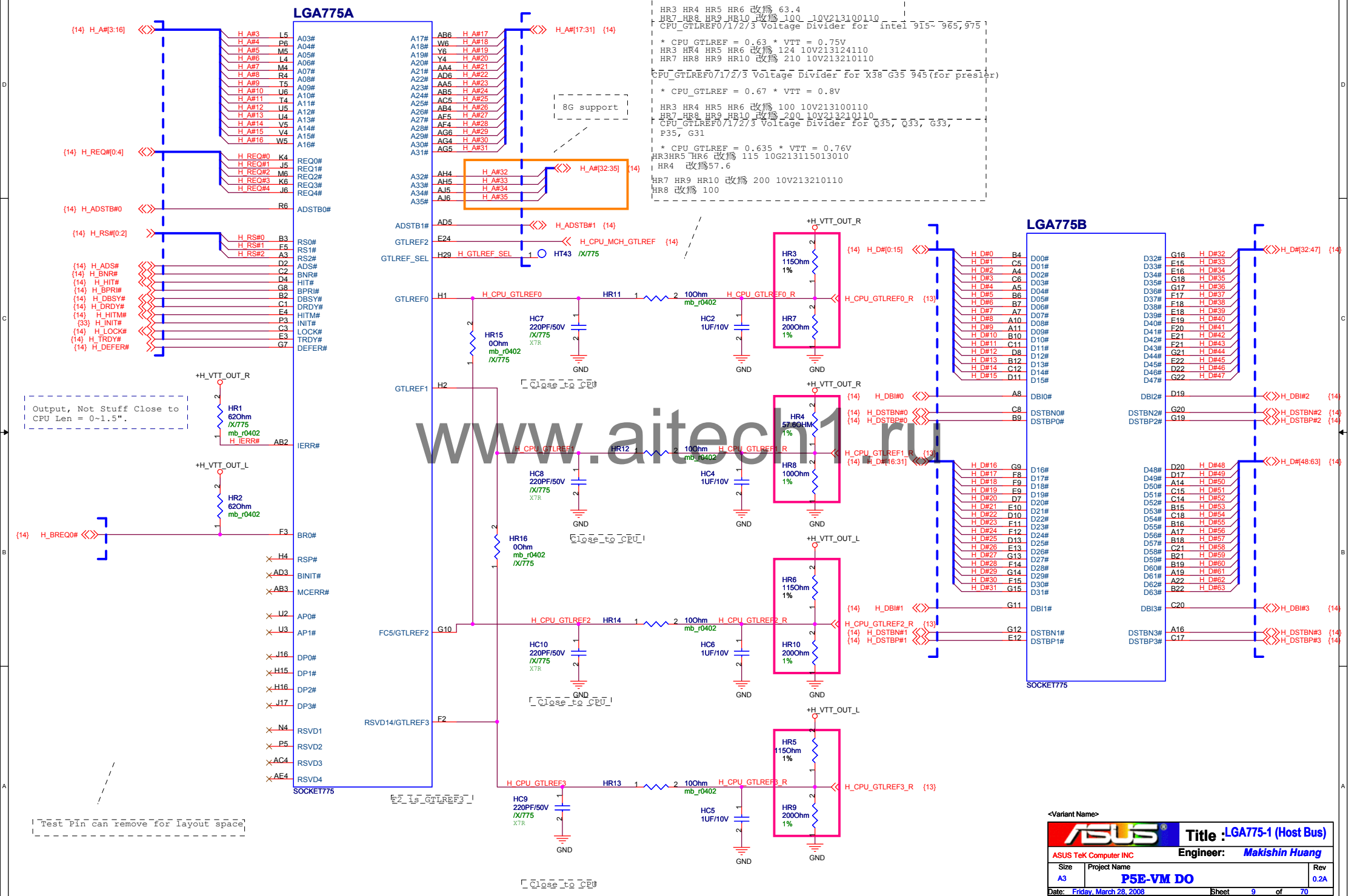


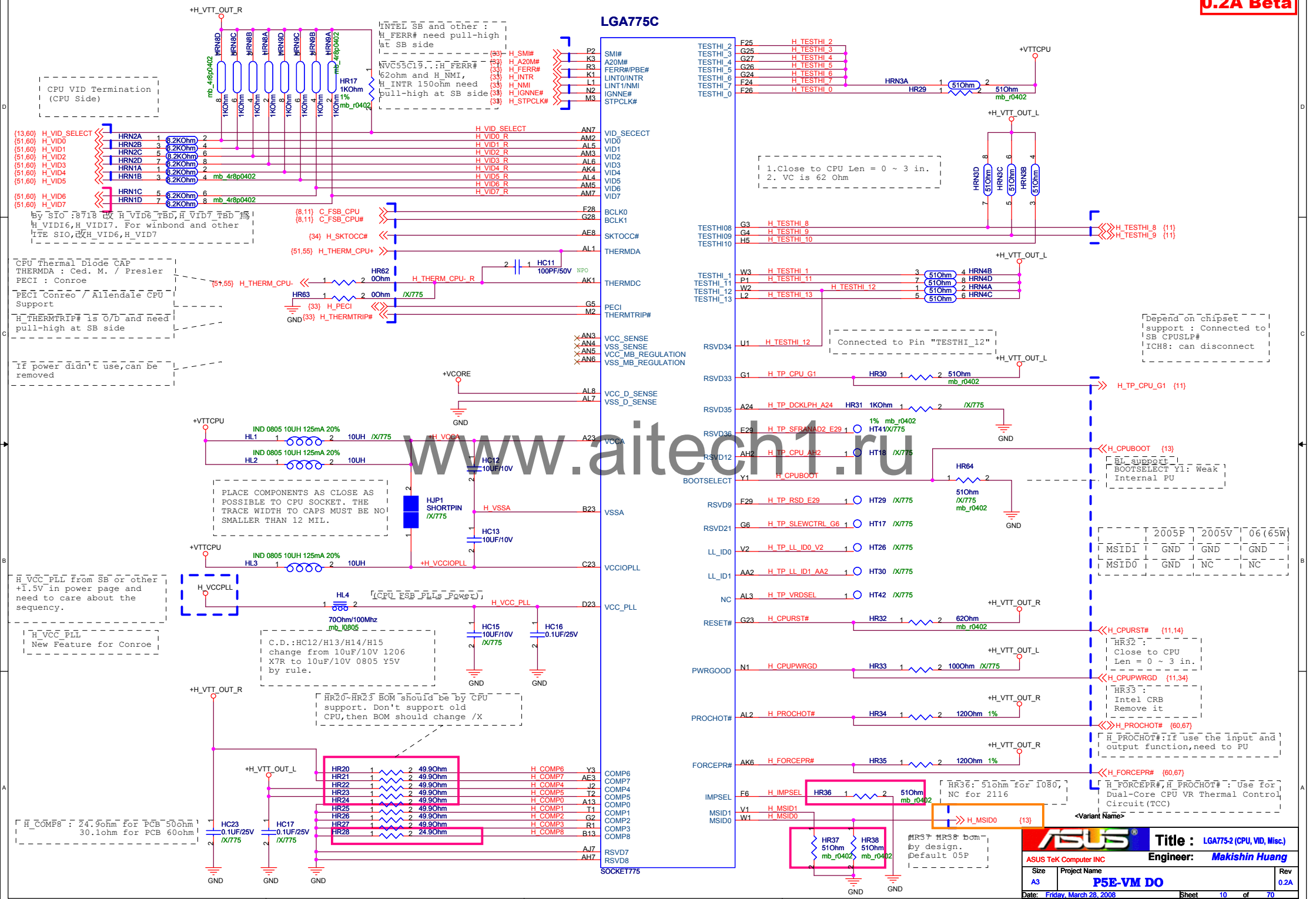


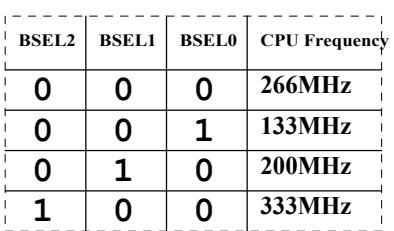
www.aitech1.ru

<Variant Name>

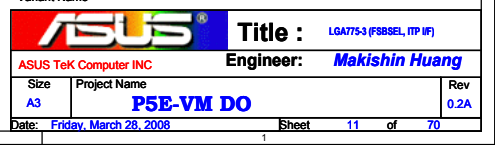
ASUS		Title : 06.Main Clock-2	
ASUSTek Computer Inc.		Engineer: Albert Chang	
Size A4	Project Name P5E-VM DO	Rev 1.00	
Date: Friday, March 28, 2008		Sheet 8 of 70	







Default 不上XDP的function
要上XDP 的CONNECTOR 的BOM 如下 請用REWORK方式
XDP HRN5 HRN6 HR44 HR46 HR51





<Variant Name>



Title : LGA775-4(POWER)

ASUS TeK Computer INC

Engineer: *Makishin Huang*

Size
A3

Project Name	
--------------	--

P5E-VM DO

Rev	
-----	--

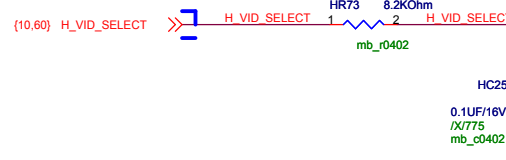
0.2A

Date: Friday, March 28, 2008

Sheet 12 of 70

	VRD10.1	VRD11
H_VID_SELECT	GND	HIGH
H_CPUBOOT	FLOATING	GND
H_MSID0	GND	FLOATING

(10,60) H_VID_SELECT



www.aitech1.ru

This table only for Q35, Q33, G33, F35, G31
Other is TBD

OV3	OV2	OV1	Ratio Set
1	1	1	0.635
	1	0	0.618
	0	1	0.597
0	0	0	0.581
	1	1	0.576
	1	0	0.561
0	0	1	0.545
	0	0	0.531

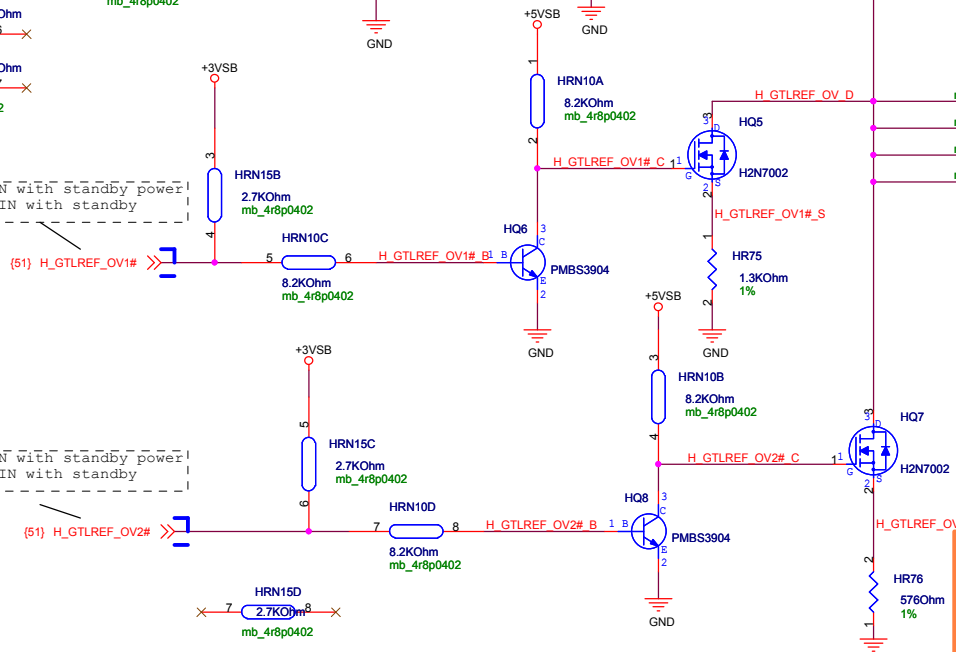
GPIO-I.Default Input PIN with standby power!
2.Default output high PIN with standby power

GPIO-I.Default Input PIN with standby power!
2.Default output high PIN with standby power

(51) H_GTLREF_OV3#

(51) H_GTLREF_OV1#

(51) H_GTLREF_OV2#



ASUS

ASUS Tek Computer INC

Size A3

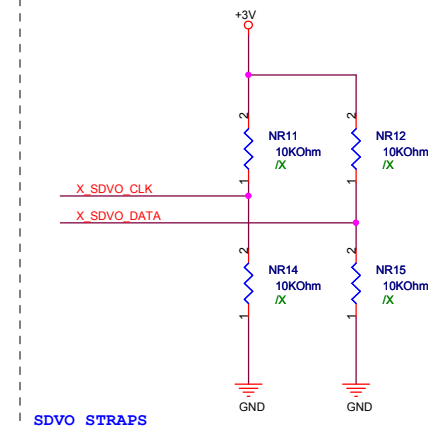
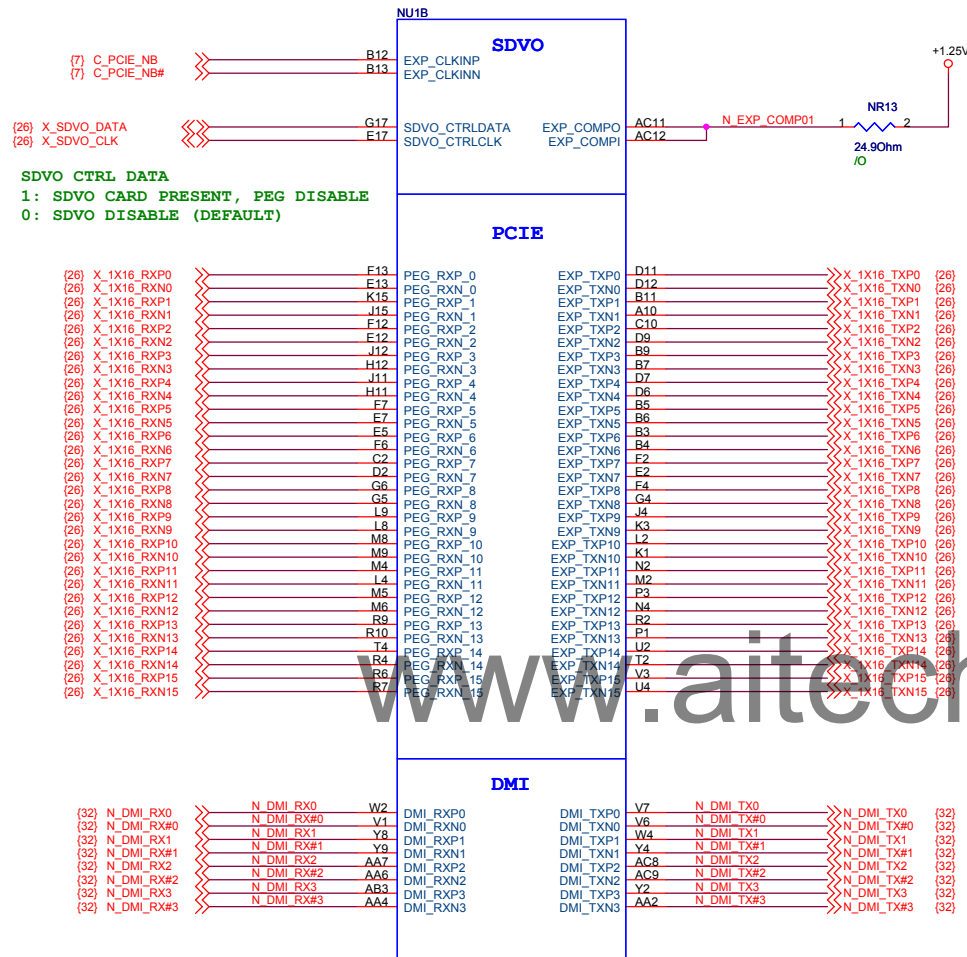
Date: Friday, March 28, 2008

Title : LGA775-5(SWITCH)

Engineer: Makishin Huang

P5E-VM DO

Sheet 13 of 70



SDVO CTRL DATA
1: SDVO CARD PRESENT, PEG DISABLE
0: SDVO DISABLE (DEFAULT)

<Variant Name>

ASUS		Title : BEARLAKE-2	
ASUSTek Computer Inc.		Engineer: Tyler_Yuan	
Size A3	Project Name P5E-VM DO	Rev 1.01G	
Date: Friday, March 28, 2008	Sheet	15	of 70

(21) D2_MAA[0..14]

(21) D2_MAA[0..14]

D2_MAA[0..14] BB30
D2_MAA1 AY25
D2_MAA2 BA23
D2_MAA3 AY23
D2_MAA4 BB22
D2_MAA5 BA22
D2_MAA6 BB21
D2_MAA7 AY21
D2_MAA8 BA21
D2_MAA9 AY21
D2_MAA10 BB31
D2_MAA11 AY21
D2_MAA12 BC20
D2_MAA13 AY38
D2_MAA14 BA19
SMA_A0
SMA_A1
SMA_A2
SMA_A3
SMA_A4
SMA_A5
SMA_A6
SMA_A7
SMA_A8
SMA_A9
SMA_A10
SMA_A11
SMA_A12
SMA_A13
SMA_A14

FOR_DDR2 BA33
AW35
AY33
SBS_A#
SCAS_A#
SRAS_A#

D2_BAA0 BA31
D2_BAA1 AY31
D2_BAA2 AY20
SBS_A0
SBS_A1
SBS_A2

D2_CS_A#0 BA34
D2_CS_A#1 AY35
D2_CS_A#2 BB33
D2_CS_A#3 BB38
SCS_A0#
SCS_A1#
SCS_A2#
SCS_A3#

D2_CKE_A0 AY19
D2_CKE_A1 AY18
D2_CKE_A2 BB19
D2_CKE_A3 BA18
SCKE_A0
SCKE_A1
SCKE_A2
SCKE_A3

D2_ODT_A0 BB35
D2_ODT_A1 BA38
D2_ODT_A2 BA35
D2_ODT_A3 BA39
SODT_A0
SODT_A1
SODT_A2
SODT_A3

D2_MA_CLK0 AR31
D2_MA_CLK0 AU31
D2_MA_CLK1 AN27
D2_MA_CLK1 AY33
D2_MA_CLK2 AW33
D2_MA_CLK2 AP29
D2_MA_CLK3 AP31
D2_MA_CLK4 AM26
D2_MA_CLK5 AM27
D2_MA_CLK5 AT33
D2_MA_CLK5 AU33
SCLK_A0
SCLK_A0#
SCLK_A1
SCLK_A1#
SCLK_A2
SCLK_A2#
SCLK_A3
SCLK_A3#
SCLK_A4
SCLK_A4#
SCLK_A5
SCLK_A5#

FOR_DDR2

FOR_DDR2

FOR_DDR2

SDQS_A0 AP2
SDQS_A0# AP3
SDM_A0 AN2
SDQ_A0 AM1
SDQ_A1 AN3
SDQ_A2 AR2
SDQ_A3 AR3
SDQ_A4 AL3
SDQ_A5 AM2
SDQ_A6 AR5
SDQ_A7 AR4
D2_DQS_A0
D2_DQS_A#0
D2_DM_A0
D2_DQ_A0
D2_DQ_A1
D2_DQ_A2
D2_DQ_A3
D2_DQ_A4
D2_DQ_A5
D2_DQ_A6
D2_DQ_A7

SDQS_A1 AW2
SDQS_A1# AW1
SDM_A1 AW3
D2_DQS_A1
D2_DQS_A#1
D2_DM_A1

SDQ_A8 AV4
SDQ_A9 AV3
SDQ_A10 BA4
SDQ_A11 BB3
SDQ_A12 AU2
SDQ_A13 AU1
SDQ_A14 AY2
SDQ_A15 AY3
D2_DQ_A8
D2_DQ_A9
D2_DQ_A10
D2_DQ_A11
D2_DQ_A12
D2_DQ_A13
D2_DQ_A14
D2_DQ_A15

SDQS_A2 AY7
SDQS_A2# BA6
SDM_A2 BB6
D2_DQS_A2
D2_DQS_A#2
D2_DM_A2

SDQ_A16 BB5
SDQ_A17 AY6
SDQ_A18 BB9
SDQ_A19 BA5
SDQ_A20 BB4
SDQ_A21 BC7
SDQ_A22 AY9
D2_DQ_A16
D2_DQ_A17
D2_DQ_A18
D2_DQ_A19
D2_DQ_A20
D2_DQ_A21
D2_DQ_A22
D2_DQ_A23

SDQS_A3 AT20
SDQS_A3# AU18
SDM_A3 AN18
D2_DQS_A3
D2_DQS_A#3
D2_DM_A3

SDQ_A24 AT18
SDQ_A25 AR18
SDQ_A26 AU21
SDQ_A27 AT21
SDQ_A28 AP17
SDQ_A29 AN17
SDQ_A30 AP20
SDQ_A31 AV20
D2_DQ_A24
D2_DQ_A25
D2_DQ_A26
D2_DQ_A27
D2_DQ_A28
D2_DQ_A29
D2_DQ_A30
D2_DQ_A31

SDQS_A4 AR41
SDQS_A4# AR40
SDM_A4 AU43
D2_DQS_A4
D2_DQS_A#4
D2_DM_A4

SDQ_A32 AV42
SDQ_A33 AU40
SDQ_A34 AP42
SDQ_A35 AP42
SDQ_A36 AV40
SDQ_A37 AV41
SDQ_A38 AR42
SDQ_A39 AP41
D2_DQ_A32
D2_DQ_A33
D2_DQ_A34
D2_DQ_A35
D2_DQ_A36
D2_DQ_A37
D2_DQ_A38
D2_DQ_A39

SDQS_A5 AL41
SDQS_A5# AL40
SDM_A5 AM43
D2_DQS_A5
D2_DQS_A#5
D2_DM_A5

SDQ_A40 AN41
SDQ_A41 AM39
SDQ_A42 AK42
SDQ_A43 AK41
SDQ_A44 AN40
SDQ_A45 AN42
SDQ_A46 AL42
SDQ_A47 AL39
D2_DQ_A40
D2_DQ_A41
D2_DQ_A42
D2_DQ_A43
D2_DQ_A44
D2_DQ_A45
D2_DQ_A46
D2_DQ_A47

SDQS_A6 AG42
SDQS_A6# AG41
SDM_A6 AG40
D2_DQS_A6
D2_DQS_A#6
D2_DM_A6

SDQ_A48 AJ40
SDQ_A49 AH43
SDQ_A50 AE39
SDQ_A51 AE40
SDQ_A52 AJ42
SDQ_A53 AJ41
SDQ_A54 AF41
SDQ_A55 AF42
D2_DQ_A48
D2_DQ_A49
D2_DQ_A50
D2_DQ_A51
D2_DQ_A52
D2_DQ_A53
D2_DQ_A54
D2_DQ_A55

SDQS_A7 AC42
SDQS_A7# AC41
SDM_A7 AC40
D2_DQS_A7
D2_DQS_A#7
D2_DM_A7

SDQ_A56 AD40
SDQ_A57 AD43
SDQ_A58 AB41
SDQ_A59 AA40
SDQ_A60 AE42
SDQ_A61 AE41
SDQ_A62 AC39
SDQ_A63 AB42
D2_DQ_A56
D2_DQ_A57
D2_DQ_A58
D2_DQ_A59
D2_DQ_A60
D2_DQ_A61
D2_DQ_A62
D2_DQ_A63

DDR_A

SMRCOMPVOH

SMRCOMPVOL

BEARLAKE

(22) D2_MAB[0..14]

D2_MAB0 AW15
D2_MAB1 BB15
D2_MAB2 BA15
D2_MAB3 AY15
D2_MAB4 BA14
D2_MAB5 BB14
D2_MAB6 AW12
D2_MAB7 BA13
D2_MAB8 BB13
D2_MAB9 AY13
D2_MAB10 BA17
D2_MAB11 AY12
D2_MAB12 BA11
D2_MAB13 AY27
D2_MAB14 BB11
SMA_B0
SMA_B1
SMA_B2
SMA_B3
SMA_B4
SMA_B5
SMA_B6
SMA_B7
SMA_B8
SMA_B9
SMA_B10
SMA_B11
SMA_B12
SMA_B13
SMA_B14

SWE_B#
SCAS_B#
SRAS_B#

SBS_B0
SBS_B1
SBS_B2

SCS_B0#
SCS_B1#
SCS_B2#
SCS_B3#

SCKE_B0
SCKE_B1
SCKE_B2
SCKE_B3

SODT_B0
SODT_B1
SODT_B2
SODT_B3

SCLK_B0
SCLK_B0#
SCLK_B1
SCLK_B1#
SCLK_B2
SCLK_B2#
SCLK_B3
SCLK_B3#
SCLK_B4
SCLK_B4#
SCLK_B5
SCLK_B5#

FOR_DDR2

FOR_DDR2

FOR_DDR2

FOR_DDR2

FOR_DDR2

FOR_DDR2

FOR_DDR2

FOR_DDR2

FOR_DDR2

FOR_DDR2

FOR_DDR2

FOR_DDR2

FOR_DDR2

SDQS_B0 AV6
SDQS_B0# AU5
SDM_B0 AR7
SDQ_B0 AN7
SDQ_B1 AN8
SDQ_B2 AW5
SDQ_B3 AW7
SDQ_B4 AN5
SDQ_B5 AN6
SDQ_B6 AN9
SDQ_B7 AU7
D2_DQS_B0
D2_DQS_B#0
D2_DM_B0
D2_DQ_B0
D2_DQ_B1
D2_DQ_B2
D2_DQ_B3
D2_DQ_B4
D2_DQ_B5
D2_DQ_B6
D2_DQ_B7

SDQS_B1 AR12
SDQS_B1# AP12
SDM_B1 AW9
D2_DQS_B1
D2_DQS_B#1
D2_DM_B1

SDQ_B8 AT11
SDQ_B9 AU11
SDQ_B10 AP13
SDQ_B11 AR13
SDQ_B12 AR11
SDQ_B13 AU9
SDQ_B14 AY12
SDQ_B15 AU12
D2_DQ_B8
D2_DQ_B9
D2_DQ_B10
D2_DQ_B11
D2_DQ_B12
D2_DQ_B13
D2_DQ_B14
D2_DQ_B15

SDQS_B2 AP15
SDQS_B2# AR15
SDM_B2 AW13
D2_DQS_B2
D2_DQS_B#2
D2_DM_B2

SDQ_B16 AU15
SDQ_B17 AV13
SDQ_B18 AU17
SDQ_B19 AT17
SDQ_B20 AU13
SDQ_B21 AW13
SDQ_B22 AV15
SDQ_B23 AW17
D2_DQ_B16
D2_DQ_B17
D2_DQ_B18
D2_DQ_B19
D2_DQ_B20
D2_DQ_B21
D2_DQ_B22
D2_DQ_B23

SDQS_B3 AT24
SDQS_B3# AU26
SDM_B3 AP23
D2_DQS_B3
D2_DQS_B#3
D2_DM_B3

SDQ_B24 AY24
SDQ_B25 AT23
SDQ_B26 AT26
SDQ_B27 AP26
SDQ_B28 AU23
SDQ_B29 AW23
SDQ_B30 AR24
SDQ_B31 AN26
D2_DQ_B24
D2_DQ_B25
D2_DQ_B26
D2_DQ_B27
D2_DQ_B28
D2_DQ_B29
D2_DQ_B30
D2_DQ_B31

SDQS_B4 AW39
SDQS_B4# AU39
SDM_B4 AU37
D2_DQS_B4
D2_DQS_B#4
D2_DM_B4

SDQ_B32 AV37
SDQ_B33 AV38
SDQ_B34 AN36
SDQ_B35 AN37
SDQ_B36 AU35
SDQ_B37 AR35
SDQ_B38 AN35
SDQ_B39 AR37
D2_DQ_B32
D2_DQ_B33
D2_DQ_B34
D2_DQ_B35
D2_DQ_B36
D2_DQ_B37
D2_DQ_B38
D2_DQ_B39

SDQS_B5 AL35
SDQS_B5# AL34
SDM_B5 AM37
D2_DQS_B5
D2_DQS_B#5
D2_DM_B5

SDQ_B40 AM35
SDQ_B41 AM38
SDQ_B42 AJ34
SDQ_B43 AL38
SDQ_B44 AR39
SDQ_B45 AM34
SDQ_B46 AL37
SDQ_B47 AL32
D2_DQ_B40
D2_DQ_B41
D2_DQ_B42
D2_DQ_B43
D2_DQ_B44
D2_DQ_B45
D2_DQ_B46
D2_DQ_B47

SDQS_B6 AG35
SDQS_B6# AG36
SDM_B6 AG39
D2_DQS_B6
D2_DQS_B#6
D2_DM_B6

SDQ_B48 AG38
SDQ_B49 AJ38
SDQ_B50 AF35
SDQ_B51 AE33
SDQ_B52 AJ37
SDQ_B53 AJ35
SDQ_B54 AG33
SDQ_B55 AF34
D2_DQ_B48
D2_DQ_B49
D2_DQ_B50
D2_DQ_B51
D2_DQ_B52
D2_DQ_B53
D2_DQ_B54
D2_DQ_B55

SDQS_B7 AC36
SDQS_B7# AC37
SDM_B7 AD38
D2_DQS_B7
D2_DQS_B#7
D2_DM_B7

SDQ_B56 AD36
SDQ_B57 AC33
SDQ_B58 AA34
SDQ_B59 AA36
SDQ_B60 AD34
SDQ_B61 AF38
SDQ_B62 AC34
SDQ_B63 AA33
D2_DQ_B56
D2_DQ_B57
D2_DQ_B58
D2_DQ_B59
D2_DQ_B60
D2_DQ_B61
D2_DQ_B62
D2_DQ_B63

BEARLAKE

DDR_B

(22) D2_DQ_B[0..63]

(22) D2_DQ_B[0..63]

SDQS_B8 AV6
SDQS_B8# AU5
SDM_B8 AR7
SDQ_B8 AN7
SDQ_B9 AN8
SDQ_B10 AW5
SDQ_B11 AW7
SDQ_B12 AN5
SDQ_B13 AN6
SDQ_B14 AN9
SDQ_B15 AU7
D2_DQS_B8
D2_DQS_B#8
D2_DM_B8
D2_DQ_B8
D2_DQ_B9
D2_DQ_B10
D2_DQ_B11
D2_DQ_B12
D2_DQ_B13
D2_DQ_B14
D2_DQ_B15

SDQS_B9 AR12
SDQS_B9# AP12
SDM_B9 AW9
D2_DQS_B9
D2_DQS_B#9
D2_DM_B9

SDQ_B16 AU15
SDQ_B17 AV13
SDQ_B18 AU17
SDQ_B19 AT17
SDQ_B20 AU13
SDQ_B21 AW13
SDQ_B22 AV15
SDQ_B23 AW17
D2_DQ_B16
D2_DQ_B17
D2_DQ_B18
D2_DQ_B19
D2_DQ_B20
D2_DQ_B21
D2_DQ_B22
D2_DQ_B23

SDQS_B10 AP15
SDQS_B10# AR15
SDM_B10 AW13
D2_DQS_B10
D2_DQS_B#10
D2_DM_B10

SDQ_B24 AY24
SDQ_B25 AT23
SDQ_B26 AT26
SDQ_B27 AP26
SDQ_B28 AU23
SDQ_B29 AW23
SDQ_B30 AR24
SDQ_B31 AN26
D2_DQ_B24
D2_DQ_B25
D2_DQ_B26
D2_DQ_B27
D2_DQ_B28
D2_DQ_B29
D2_DQ_B30
D2_DQ_B31

SDQS_B11 AT24
SDQS_B11# AU26
SDM_B11 AP23
D2_DQS_B11
D2_DQS_B#11
D2_DM_B11

SDQ_B32 AV37
SDQ_B33 AV38
SDQ_B34 AN36
SDQ_B35 AN37
SDQ_B36 AU35
SDQ_B37 AR35
SDQ_B38 AN35
SDQ_B39 AR37
D2_DQ_B32
D2_DQ_B33
D2_DQ_B34
D2_DQ_B35
D2_DQ_B36
D2_DQ_B37
D2_DQ_B38
D2_DQ_B39

SDQS_B12 AL35
SDQS_B12# AL34
SDM_B12 AM37
D2_DQS_B12
D2_DQS_B#12
D2_DM_B12

SDQ_B40 AM35
SDQ_B41 AM38
SDQ_B42 AJ34
SDQ_B43 AL38
SDQ_B44 AR39
SDQ_B45 AM34
SDQ_B46 AL37
SDQ_B47 AL32
D2_DQ_B40
D2_DQ_B41
D2_DQ_B42
D2_DQ_B43
D2_DQ_B44
D2_DQ_B45
D2_DQ_B46
D2_DQ_B47

SDQS_B13 AG35
SDQS_B13# AG36
SDM_B13 AG39
D2_DQS_B13
D2_DQS_B#13
D2_DM_B13

SDQ_B48 AG38
SDQ_B49 AJ38
SDQ_B50 AF35
SDQ_B51 AE33
SDQ_B52 AJ37
SDQ_B53 AJ35
SDQ_B54 AG33
SDQ_B55 AF34
D2_DQ_B48
D2_DQ_B49
D2_DQ_B50
D2_DQ_B51
D2_DQ_B52
D2_DQ_B53
D2_DQ_B54
D2_DQ_B55

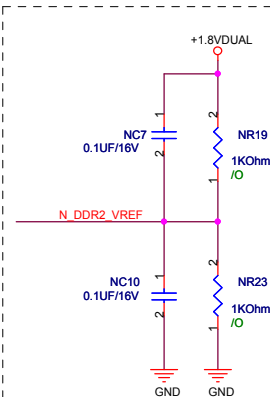
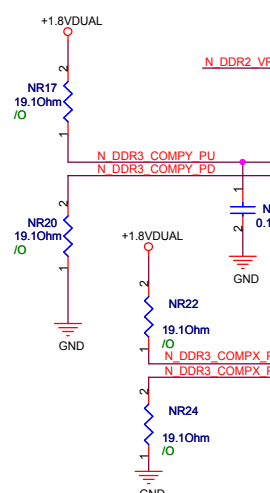
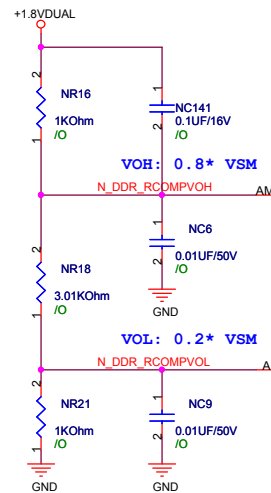
SDQS_B14 AC36
SDQS_B14# AC37
SDM_B14 AD38
D2_DQS_B14
D2_DQS_B#14
D2_DM_B14

SDQ_B56 AD36
SDQ_B57 AC33
SDQ_B58 AA34
SDQ_B59 AA36
SDQ_B60 AD34
SDQ_B61 AF38
SDQ_B62 AC34
SDQ_B63 AA33
D2_DQ_B56
D2_DQ_B57
D2_DQ_B58
D2_DQ_B59
D2_DQ_B60
D2_DQ_B61
D2_DQ_B62
D2_DQ_B63

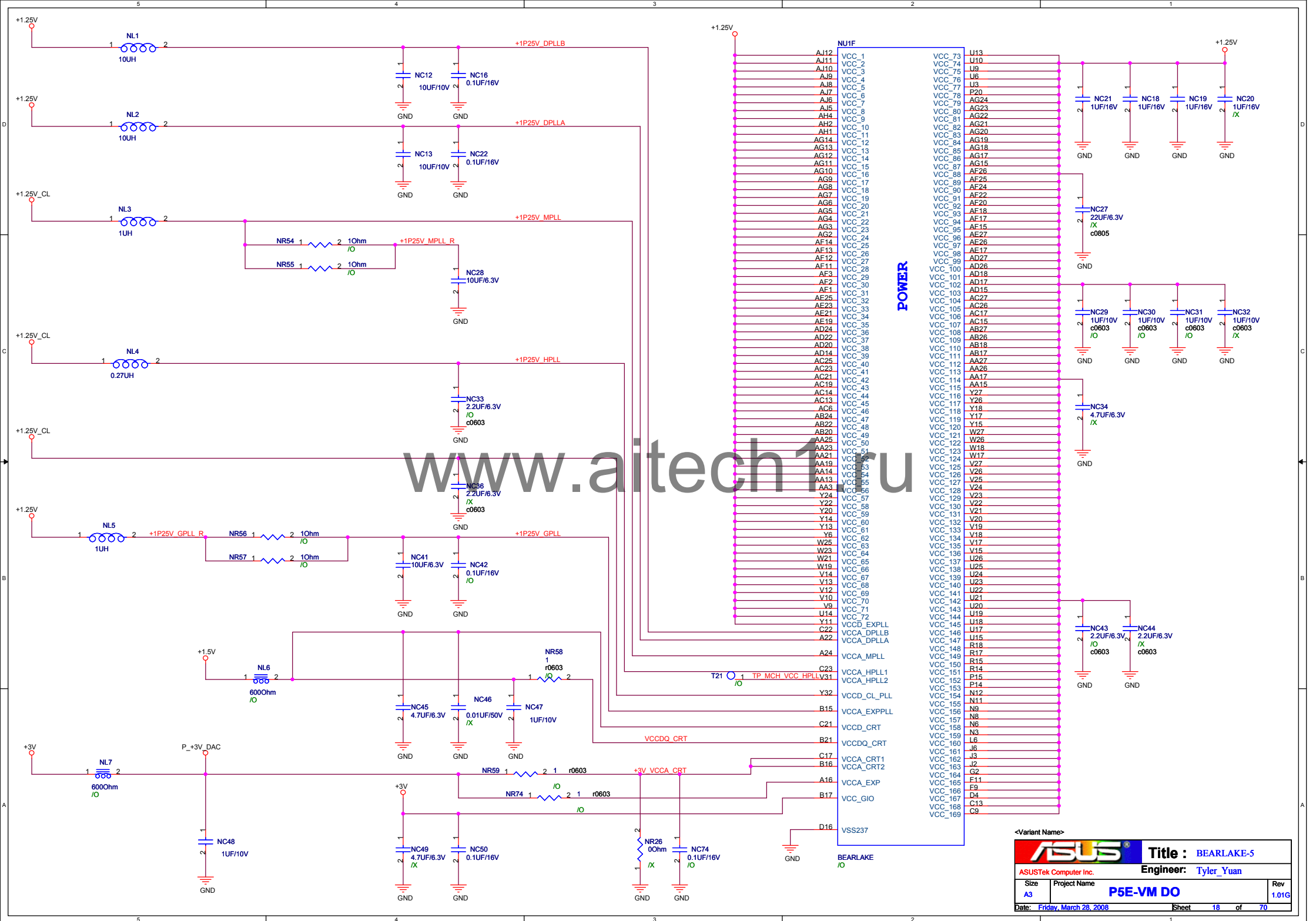
SDQS_B15 AT24
SDQS_B15# AU26
SDM_B15 AP23
D2_DQS_B15
D2_DQS_B#15
D2_DM_B15

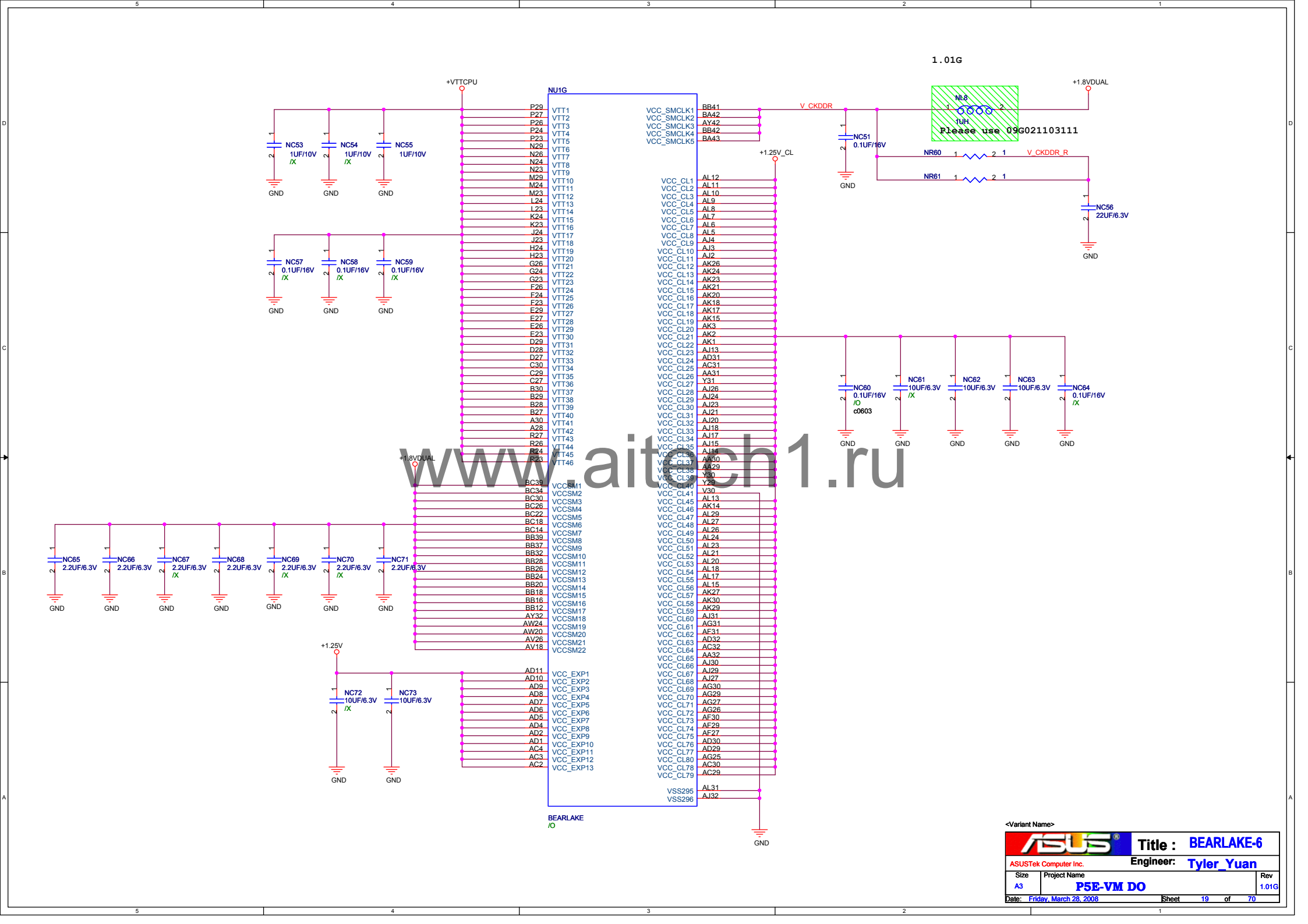
SDQ_B60 AM35
SDQ_B61 AM38
SDQ_B62 AJ34
SDQ_B63 AL38
SDQ_B64 AR39
SDQ_B65 AM34
SDQ_B66 AL37
SDQ_B67 AL32
D2_DQ_B60
D2_DQ_B61
D2_DQ_B62
D2_DQ_B63
D2_DQ_B64
D2_DQ_B65
D2_DQ_B66
D2_DQ_B67

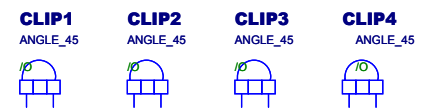
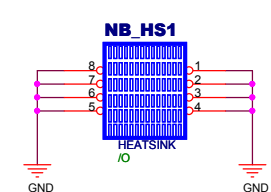
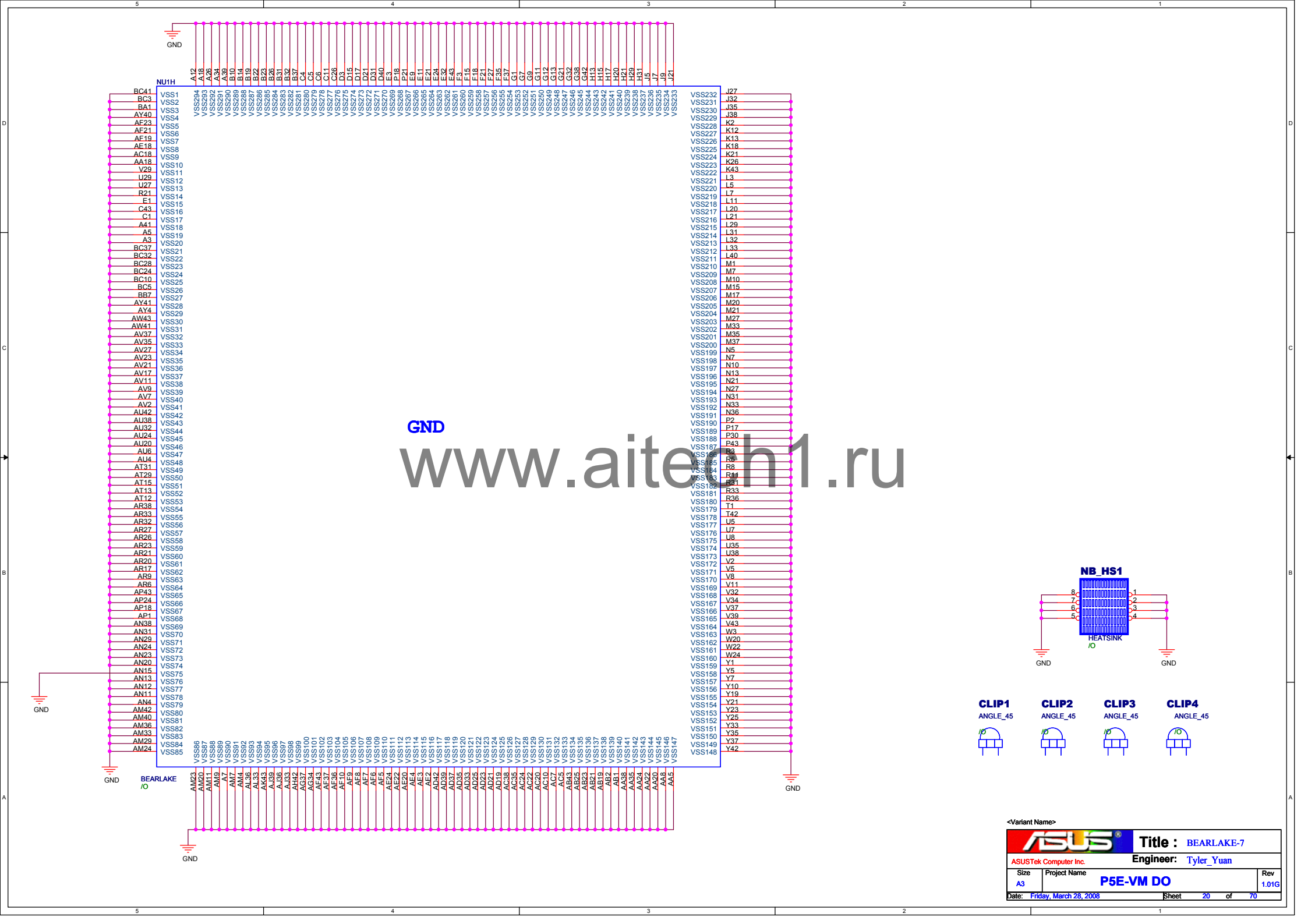
BEARLAKE



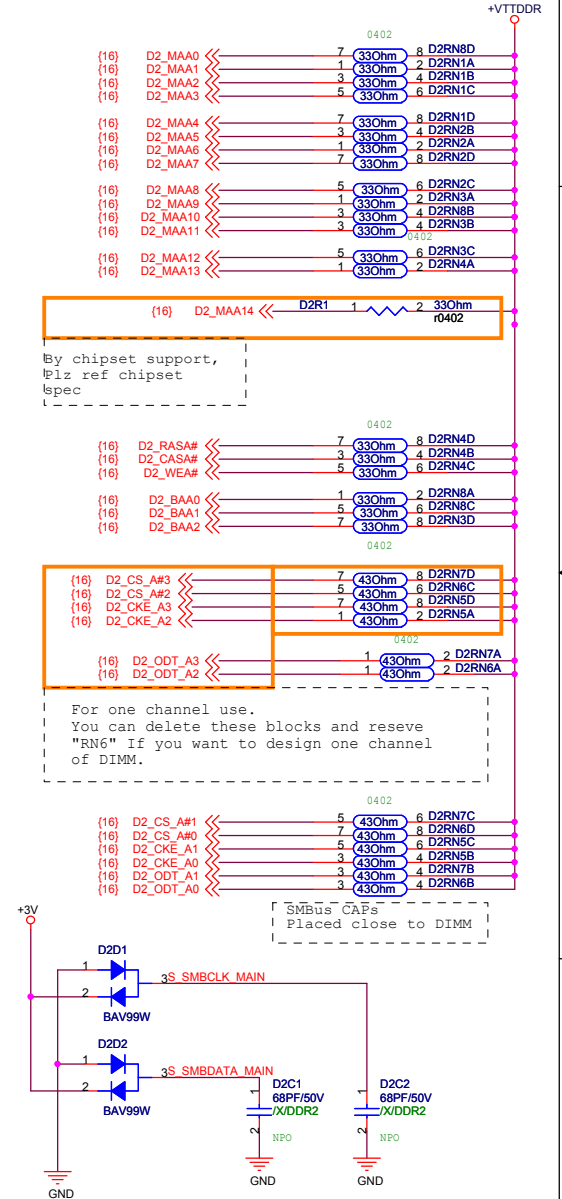
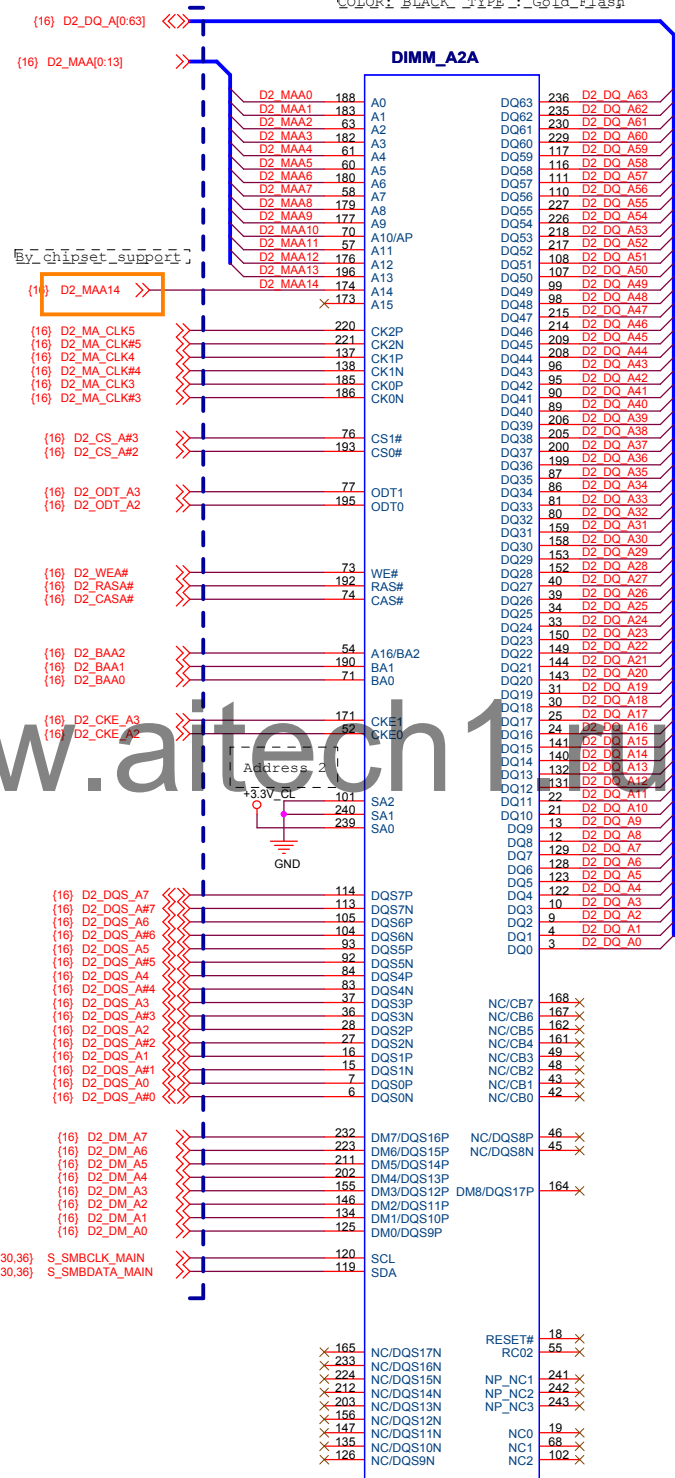
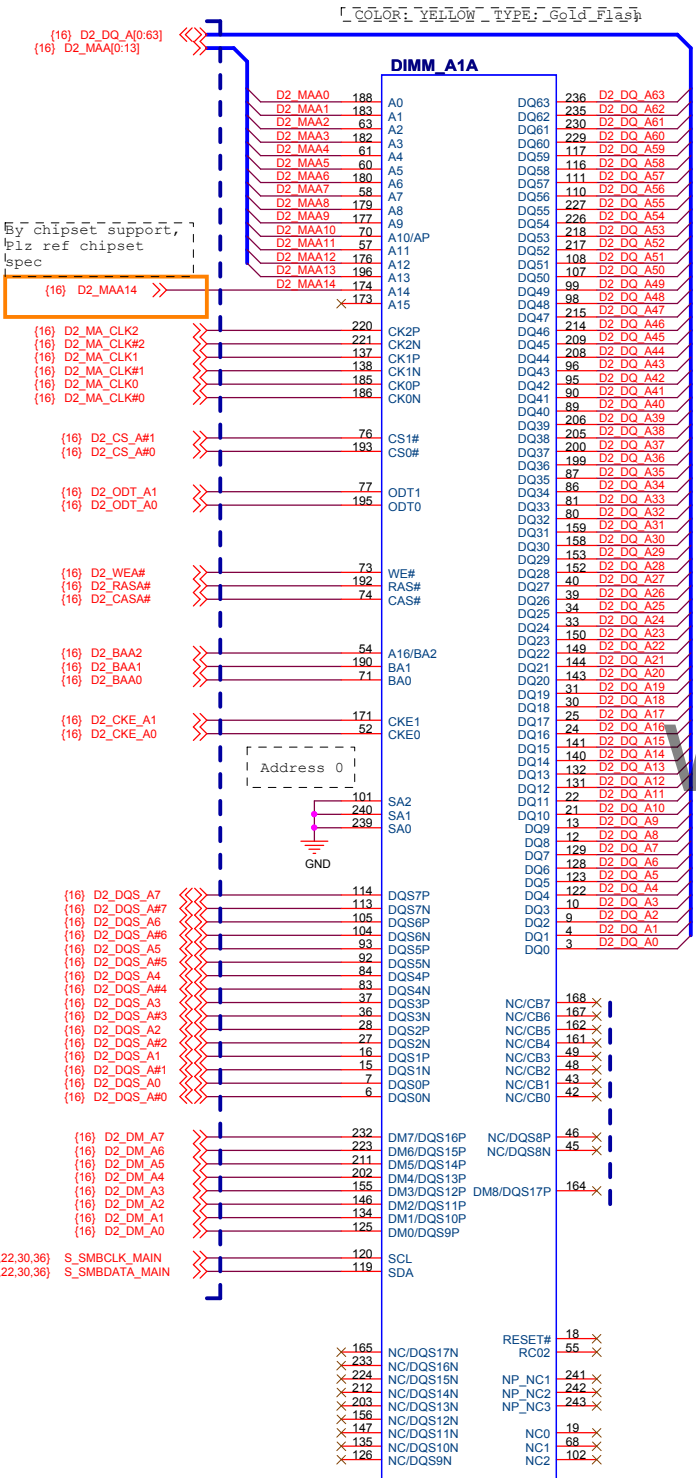
ASUS
Title : BEARLAKE-3
Engineer: Tyler Yuan
Size A3 Project Name P5E-VM DO Rev 1.0IG
Date: Friday, March 28, 2008 Sheet 16 of 70

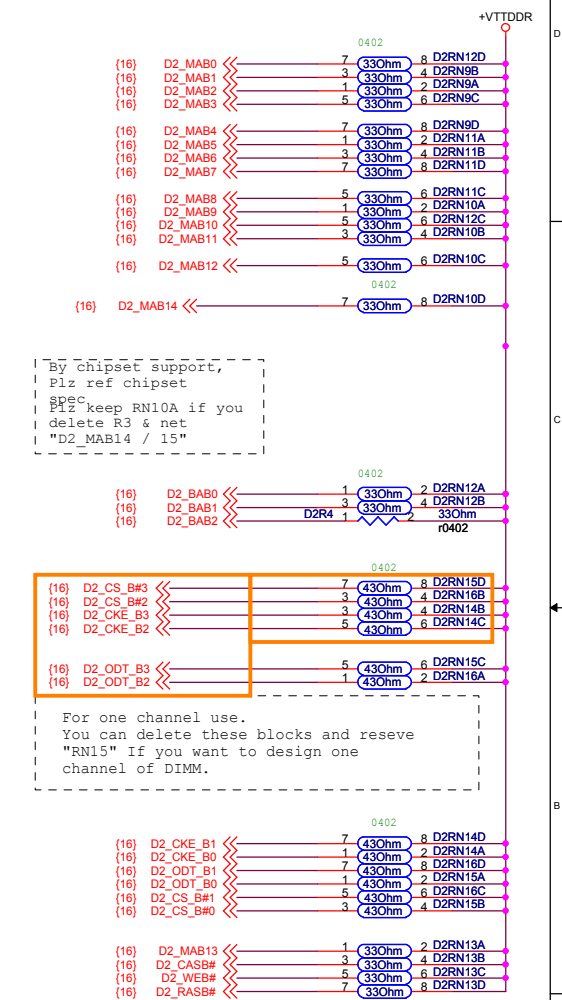
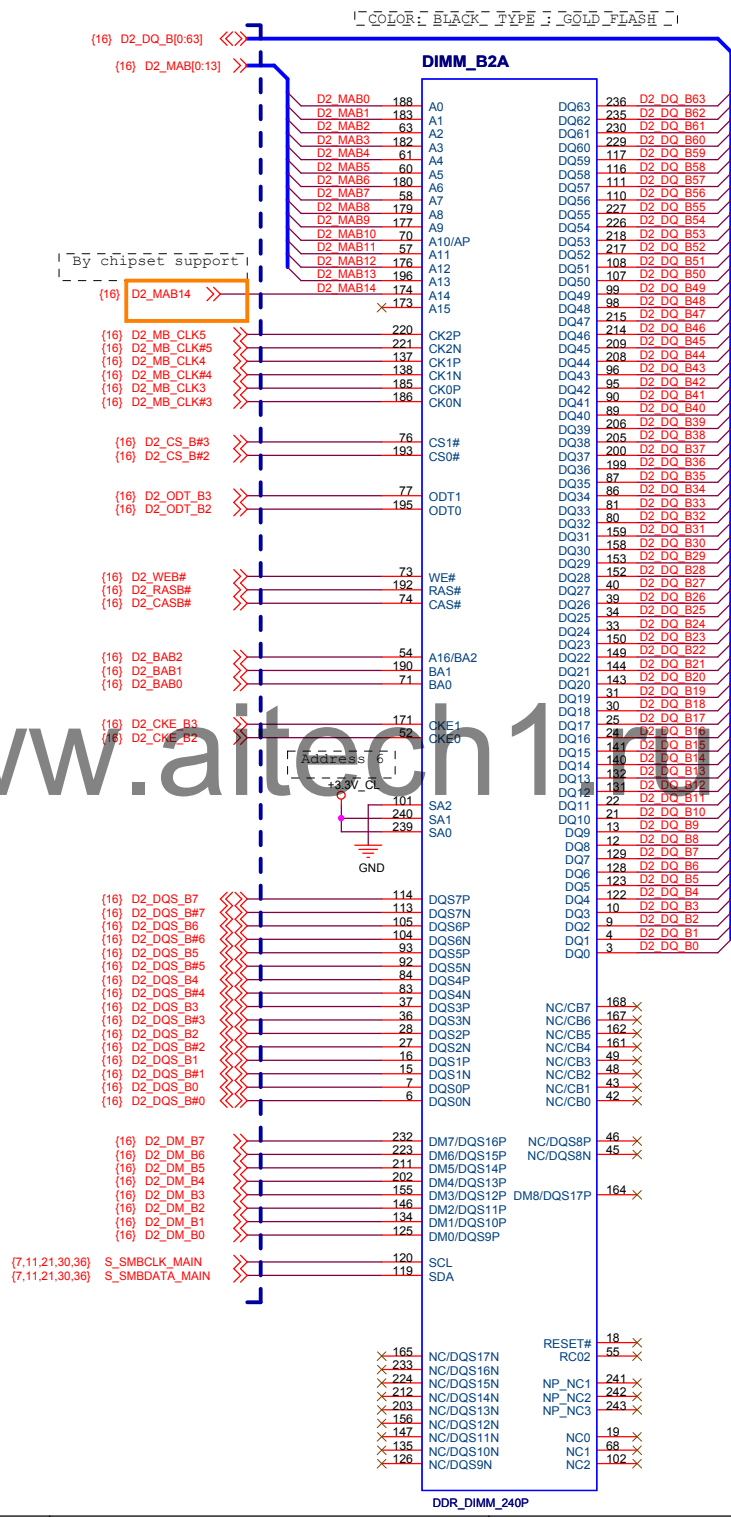


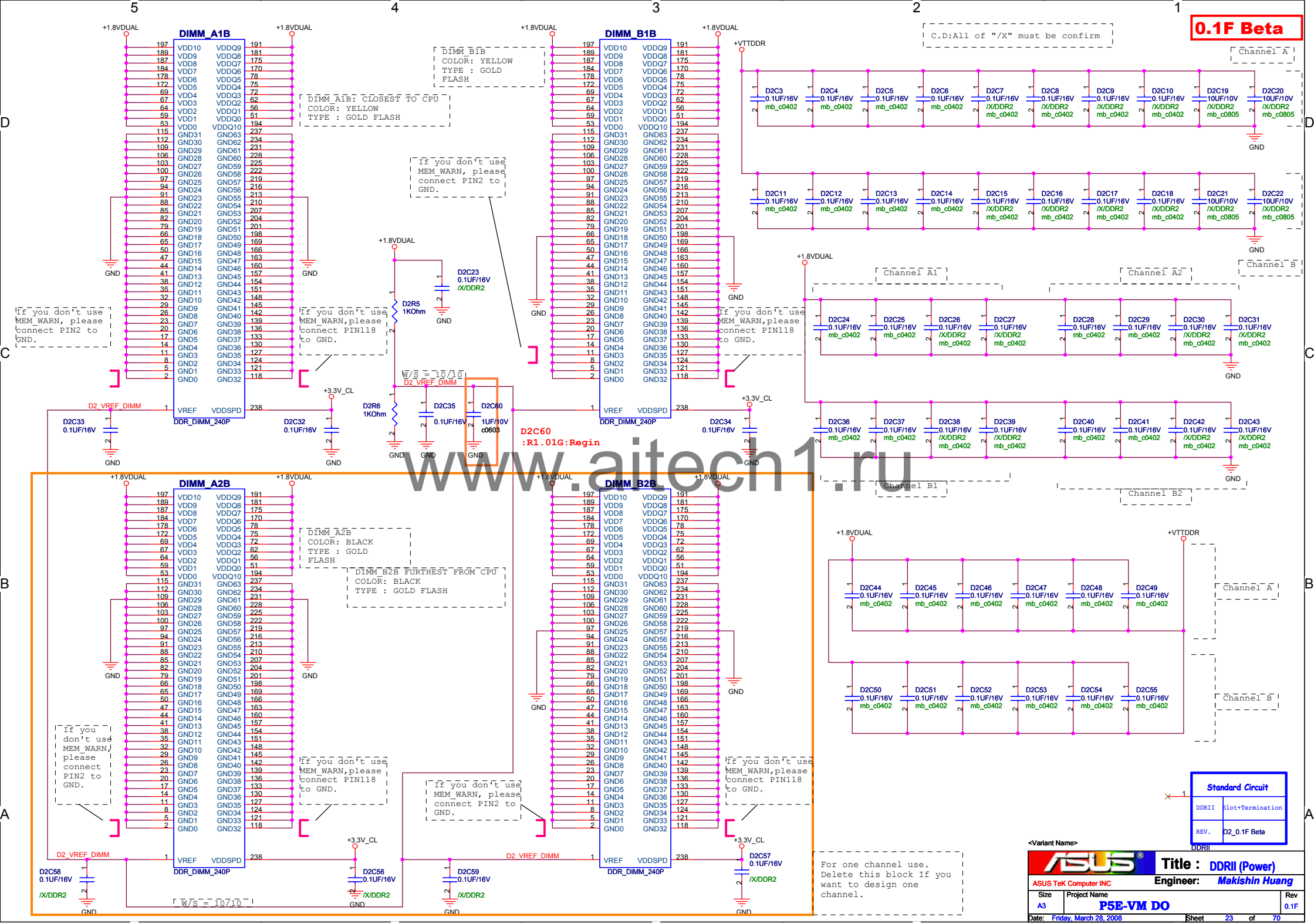




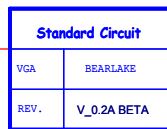
For one channel use.
Delete this block if you
want to design one
channel.





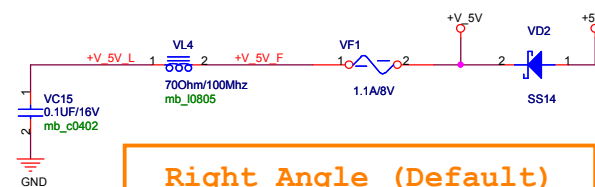
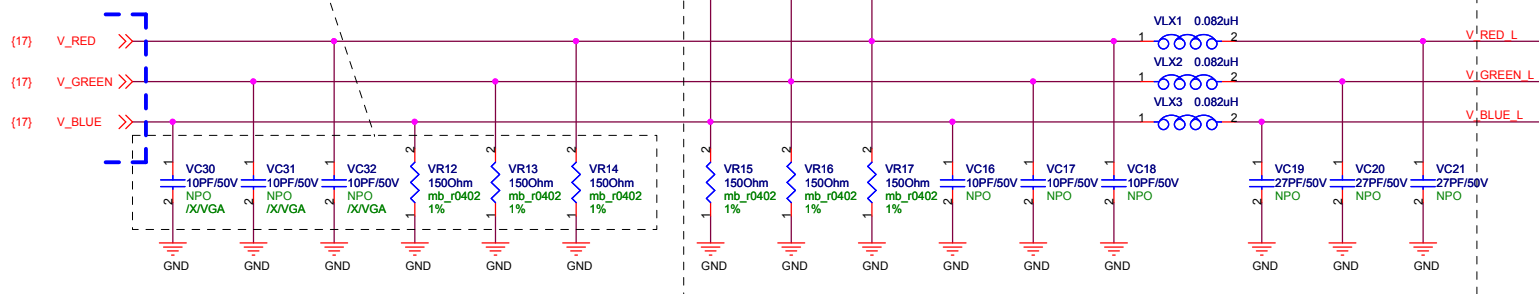


For Intel Bearlake Chipset

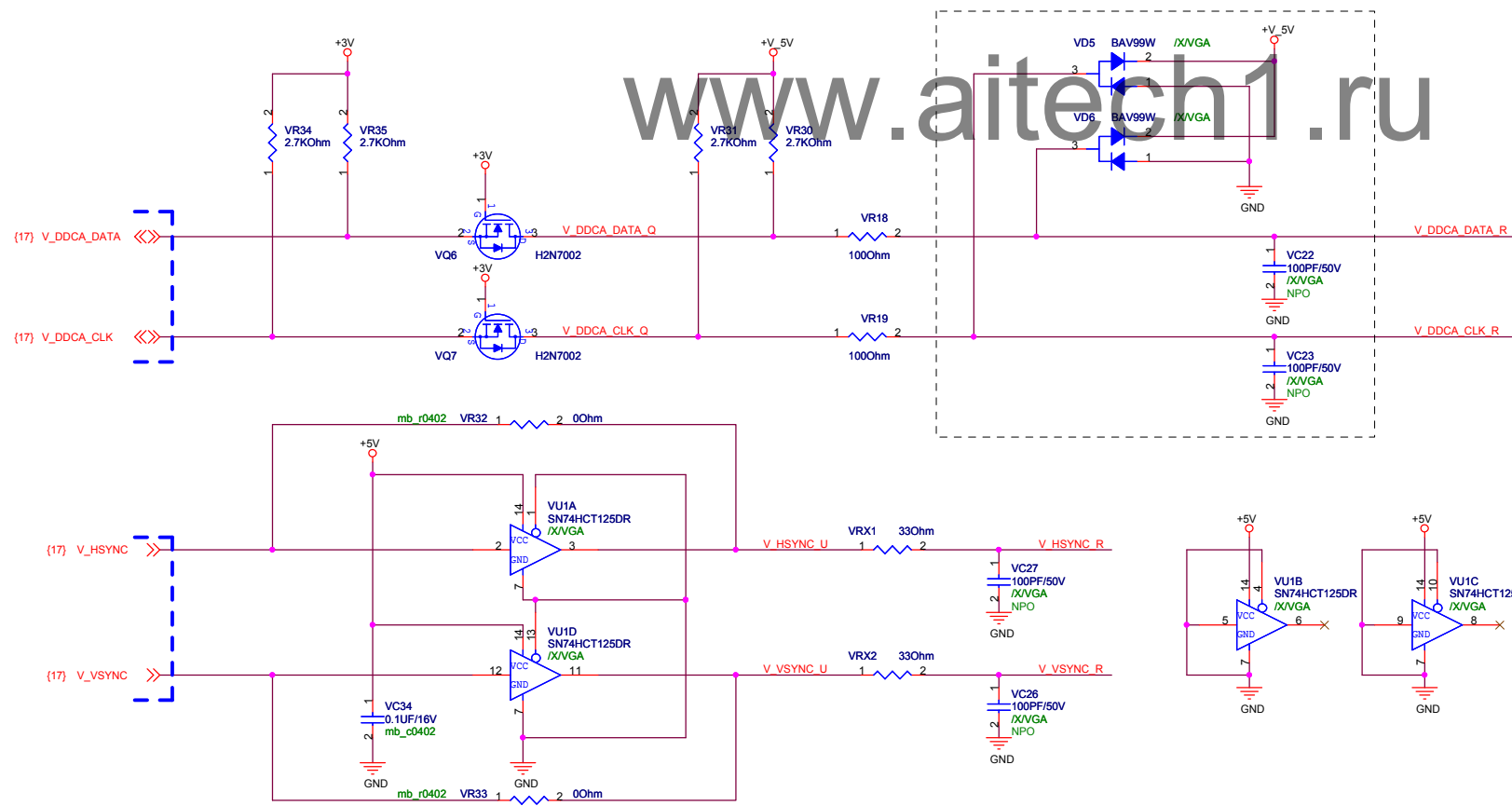
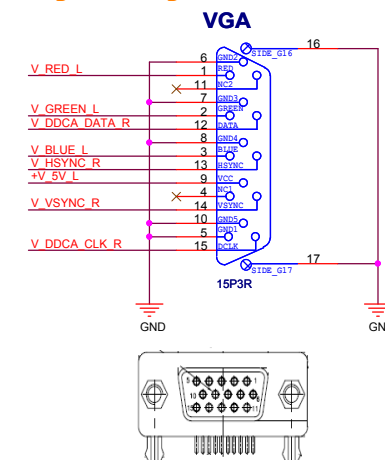


Place near connector side

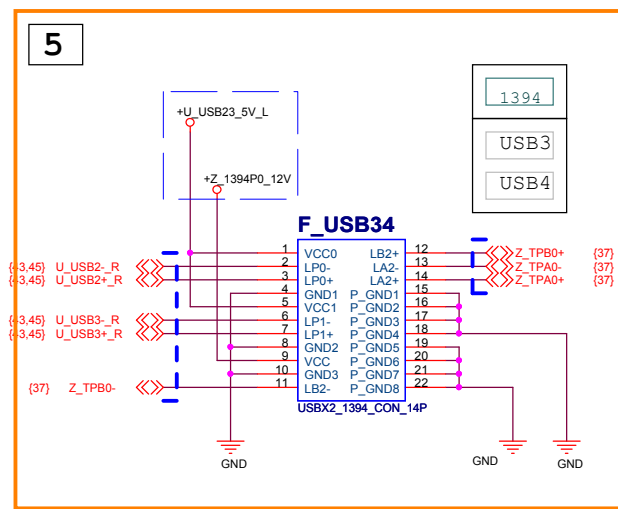
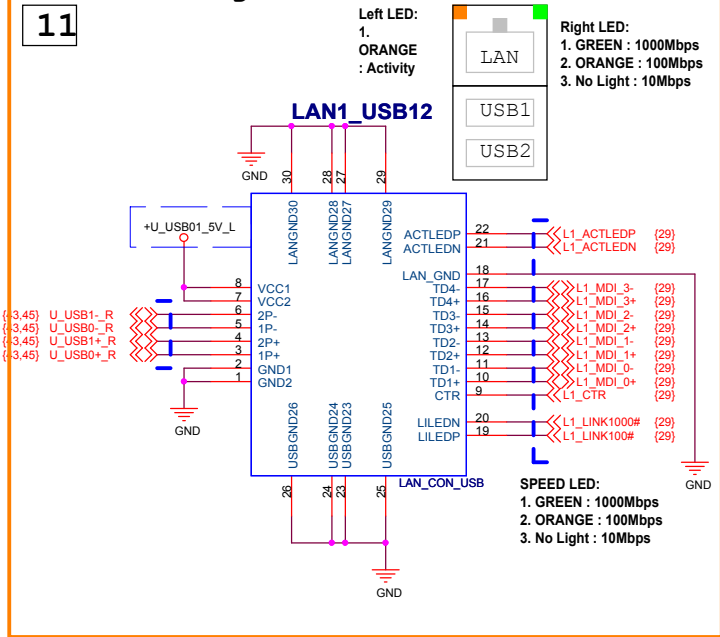
Place near NB side



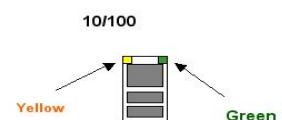
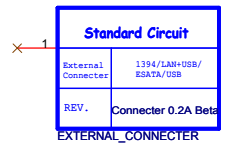
Right Angle (Default)



1.For single GIGA LAN1



www.aitech1.ru



Lan chip	Yellow (Left)	Green (Right)
Phy Realtek RTL8201 series	100M Activity	10M Activity
Phy VIA VT6103 series	On: 100M Link Off: 10M Link	Activity
Recommended design	Activity	On: 100M Link Off: 10M Link

<Variant Name>

ASUS Title : **Connector2**

ASUSTEK Computer INC Engineer: **Makishin_Huang**

Size A3 Project Name **P5E-VM DO** Rev 0.2A

Date: Friday, March 28, 2008 Sheet 25 of 70

PCIEX16_1

若無使用SLOT_WARN線路，
請將X_1X16_DET_A接至GND。

X_WAKE# 需在SB端Pull-high

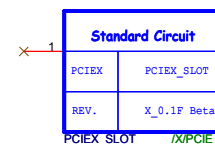
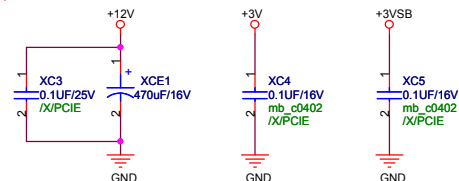
(1)
如有使用，需在SB端
以8.2K OhmPull
high至+3V。

(2)
若不使用，請RD將其
接至GND，不能
floating，並請確認
SB是否需要Pull
high or pull
down。

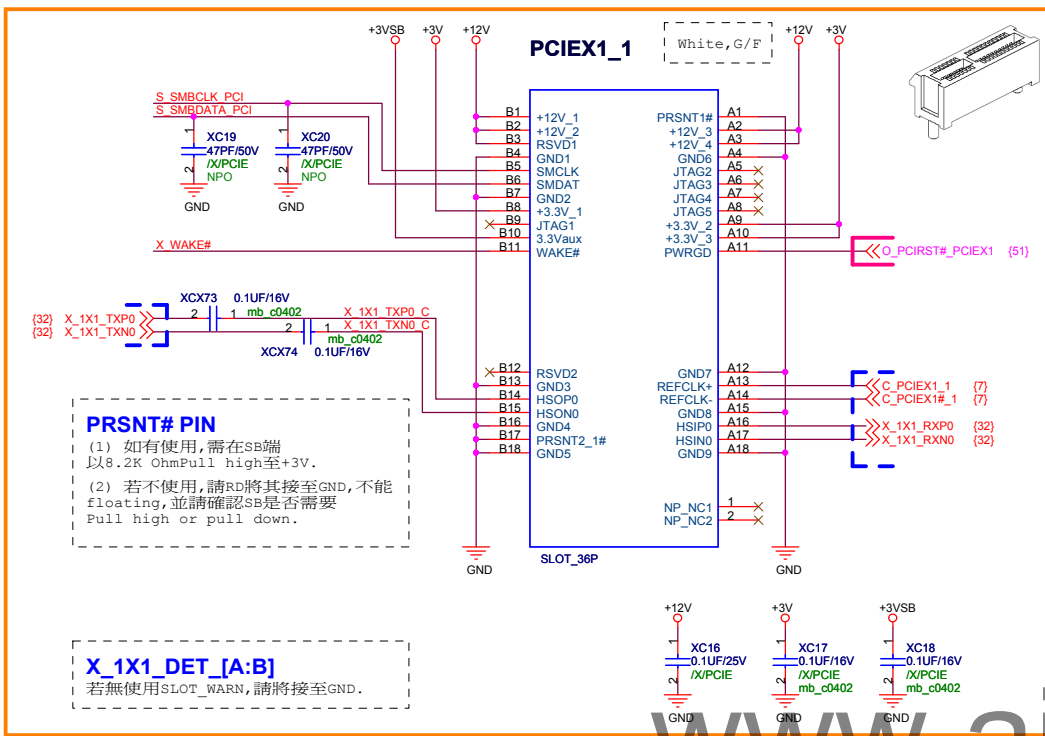
(3)
若Chipset有support
SDVO，請RD自行修改
Netname。沒有使用的
Net請接至GND，不能
floating。

若無使用SLOT_WARN線路，
請將X_1X16_DET_[A:B]接至GND。

Default :Blue,G/F,Latch往上
若要使用15U的SLOT，
請RD自行更換
料號：12V306164UU2

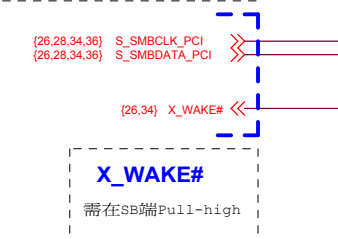


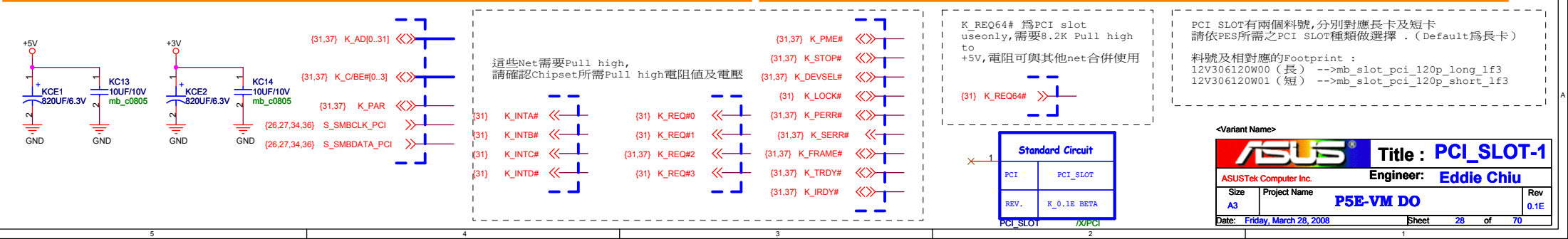
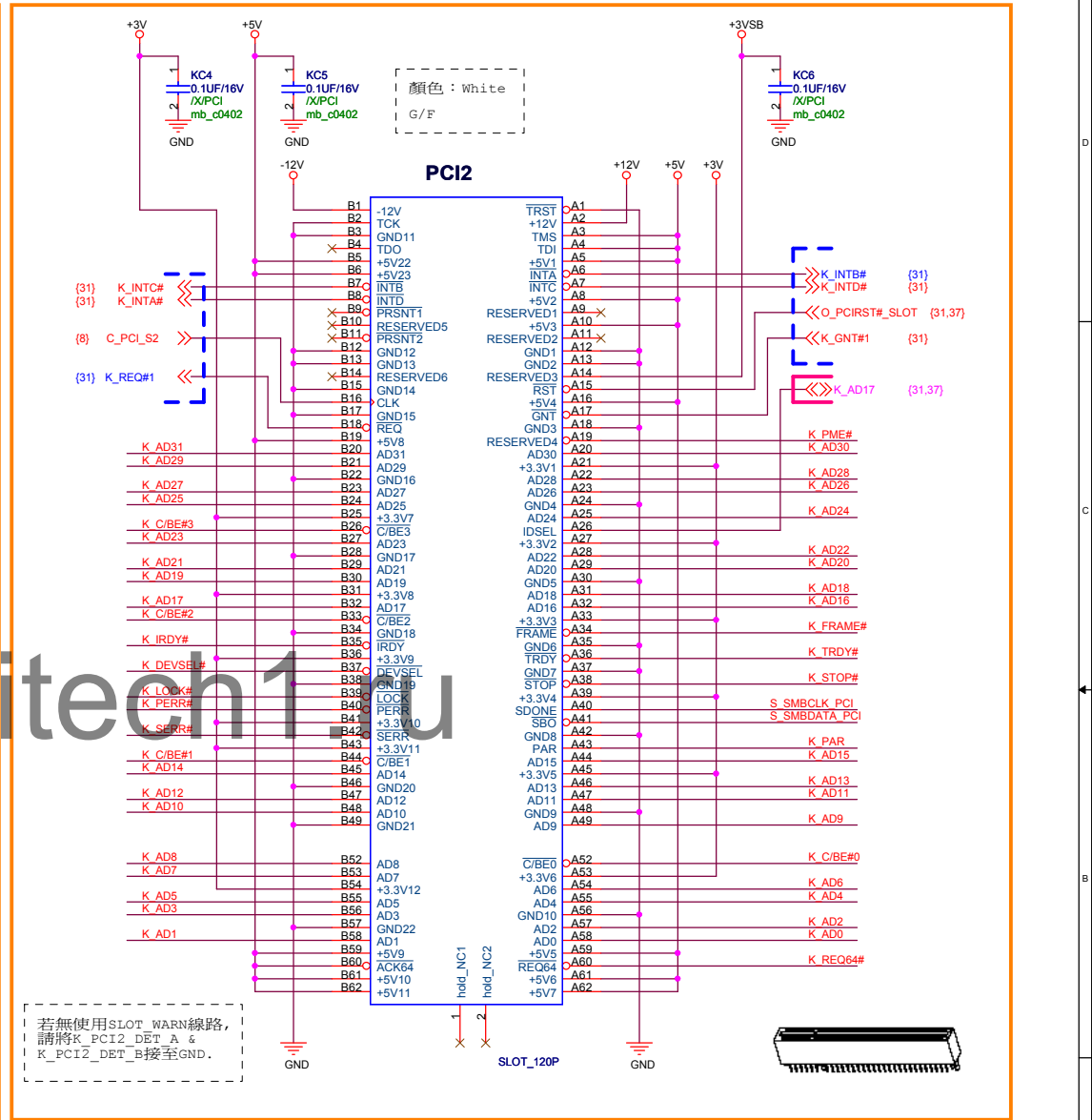
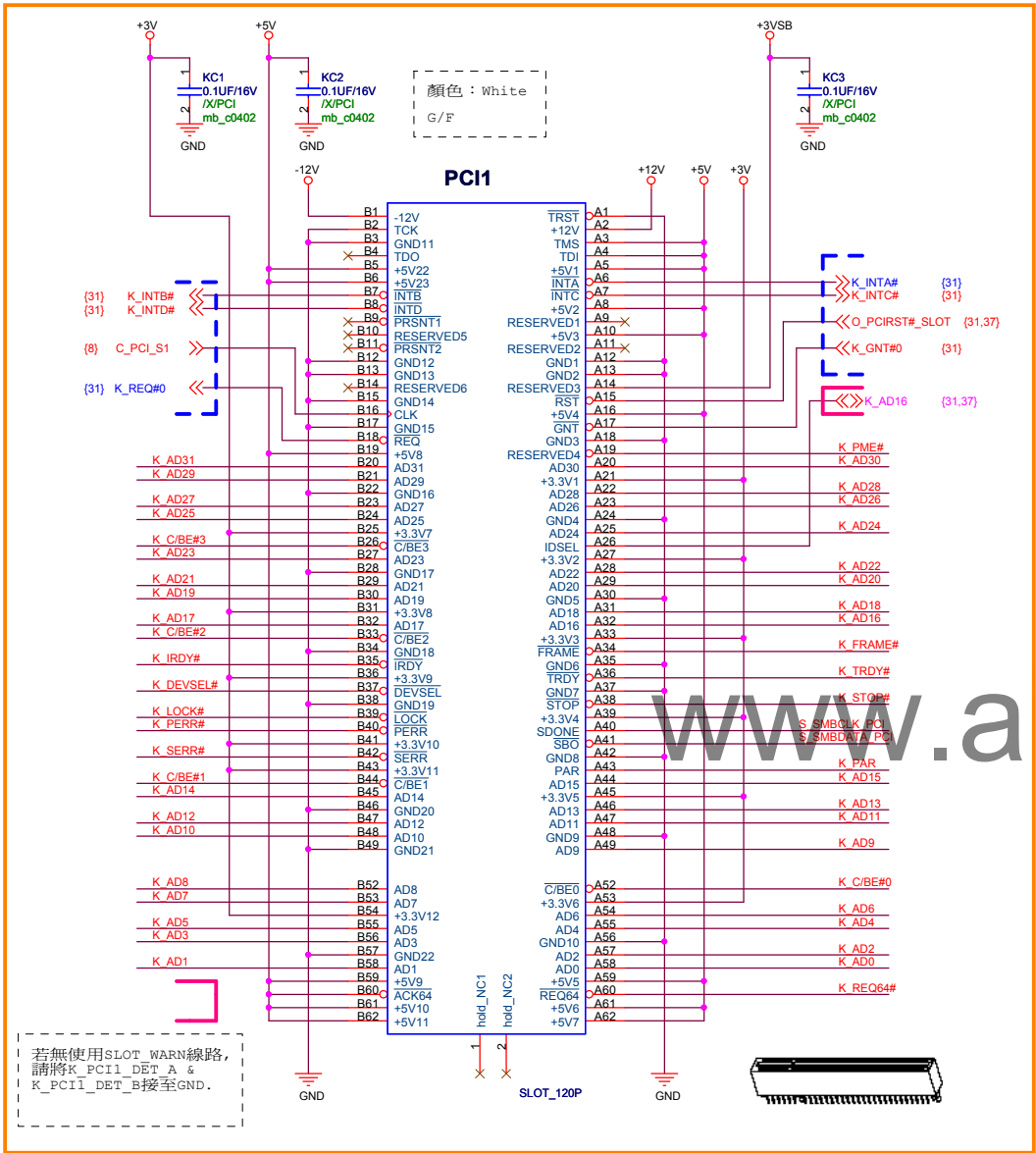
<Variant Name>



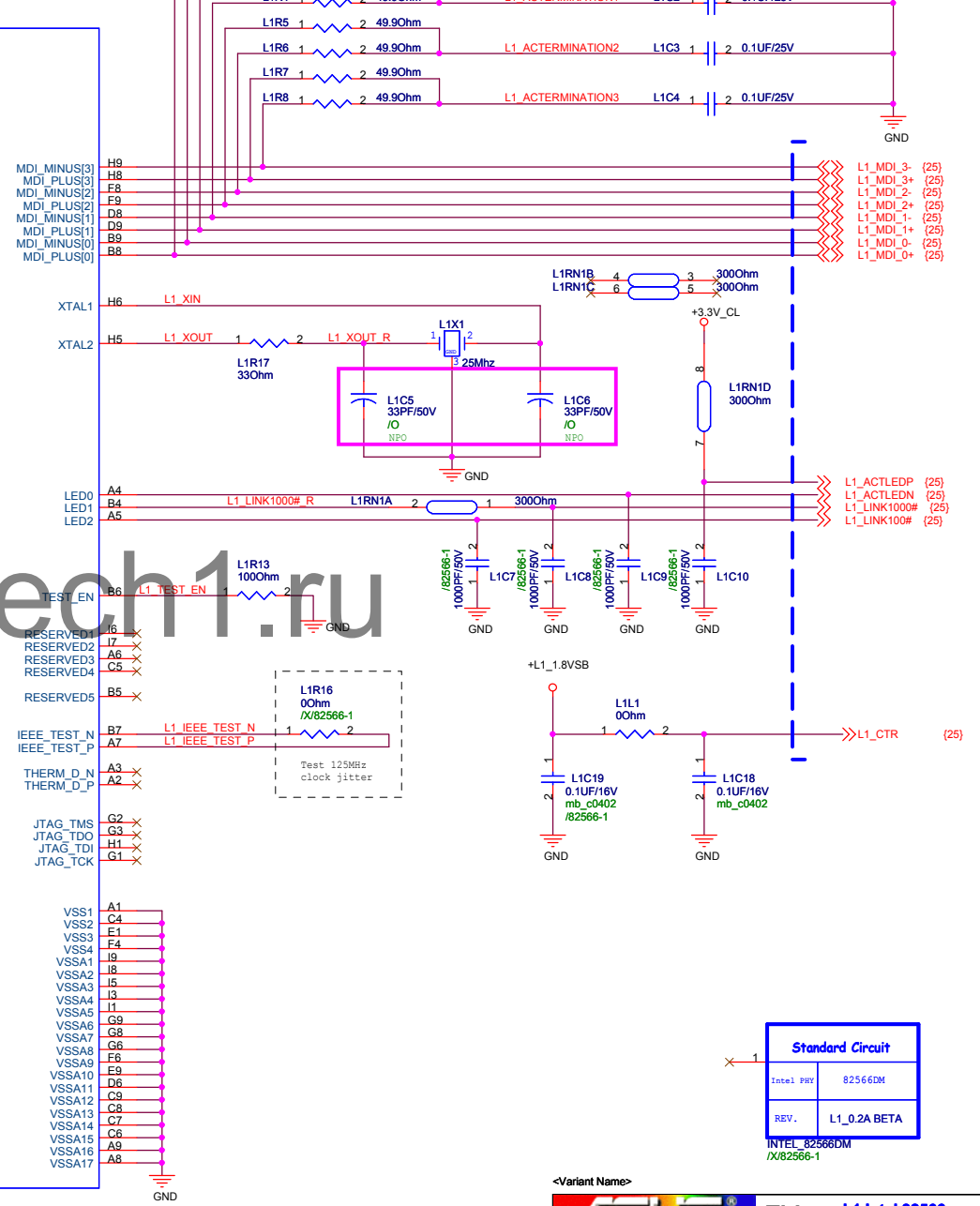
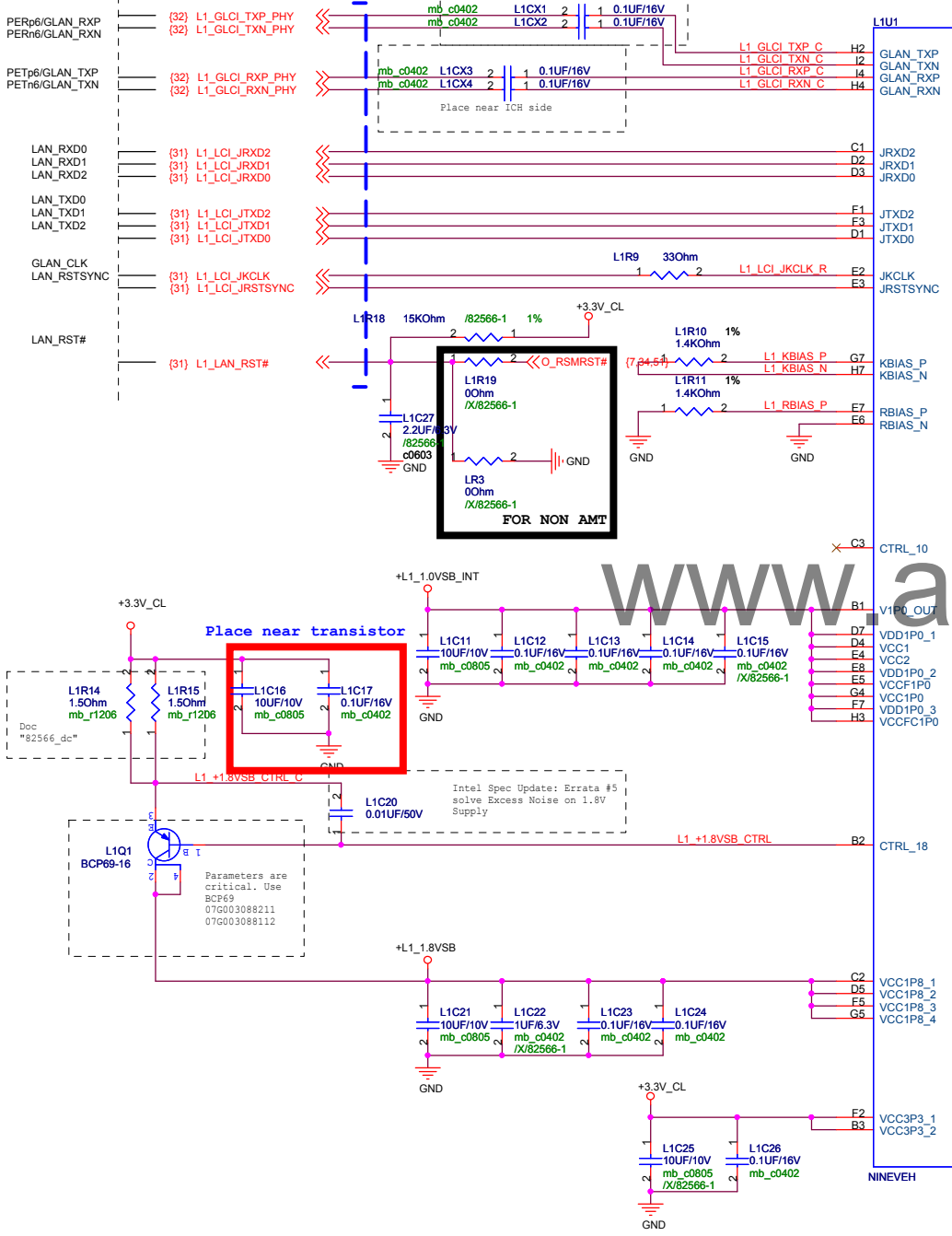
www.aitech1.ru

**S_SMBCLK_PCI &
S_SMBDATA_PCI**
需接至SB SMBus (吃standby
power)





ICH side

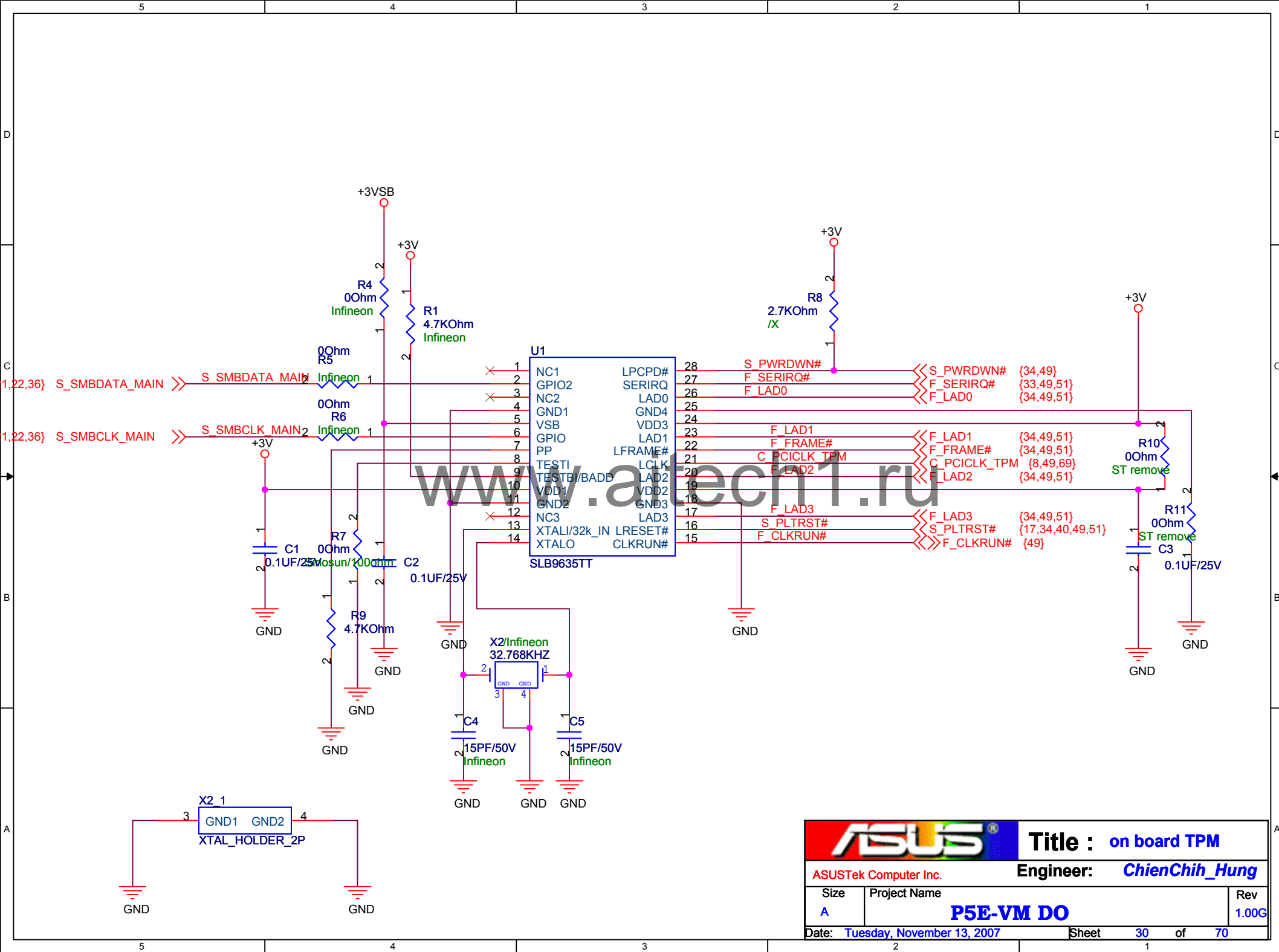


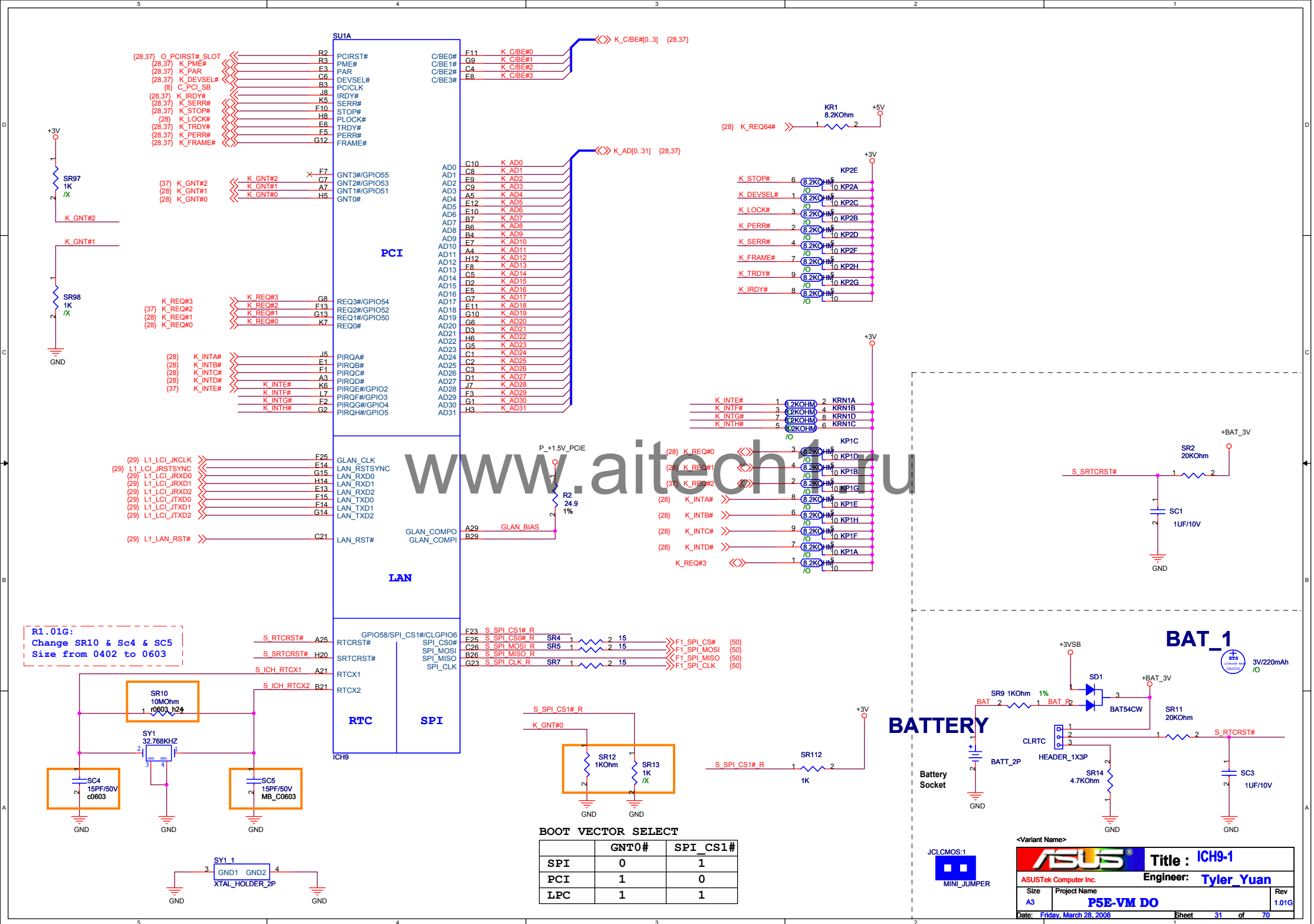
www.aitech1.ru

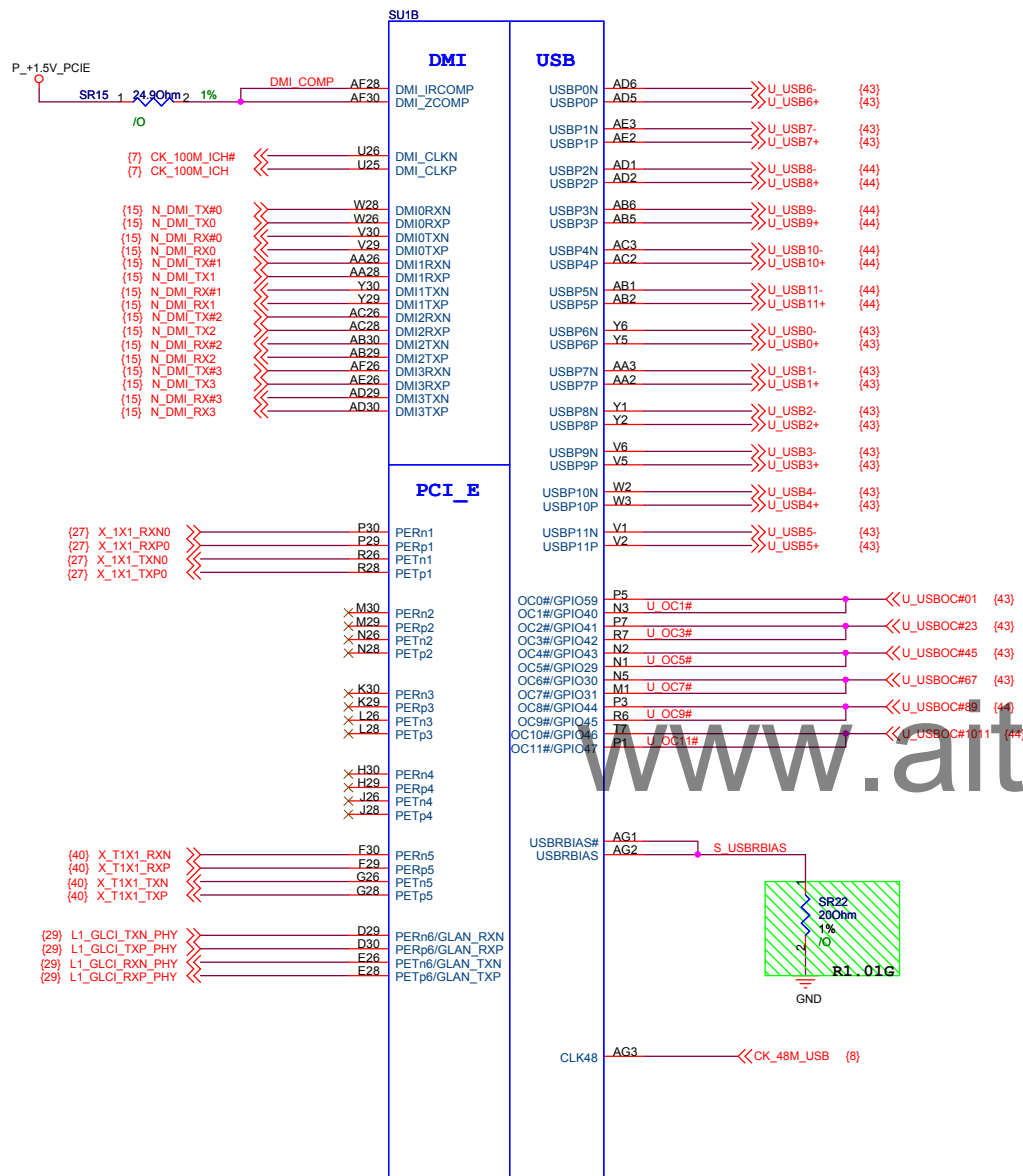
Standard Circuit	
Intel PHY	82566DM
REV.	L1_0.2A BETA

<Variant Name>

		Title : L1 Intel 82566	
ASUSTek Computer Inc.		Engineer: Nick Kao	
Size	Project Name	P5E-VM DO	
A3		Rev 0.1A	
Date:	Friday, March 28, 2008	Sheet	29 of 70



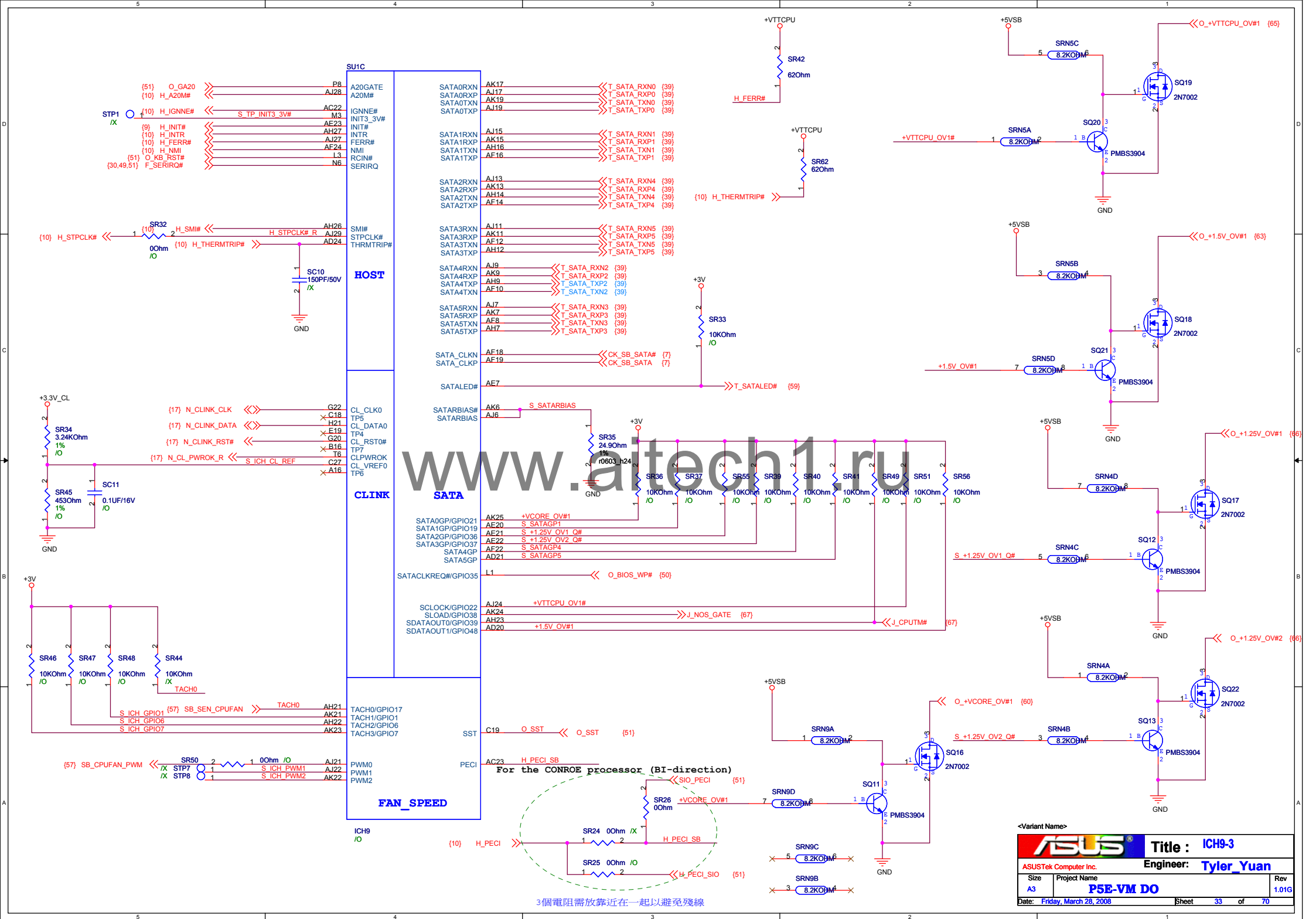


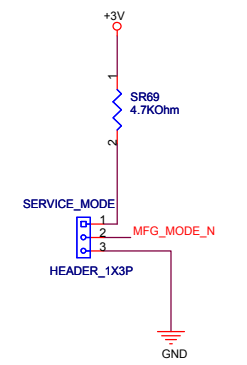
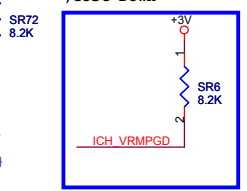
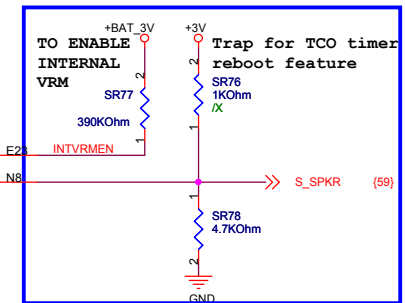
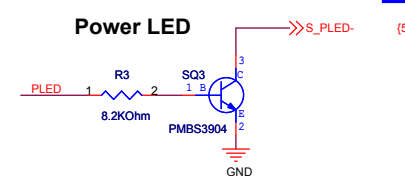
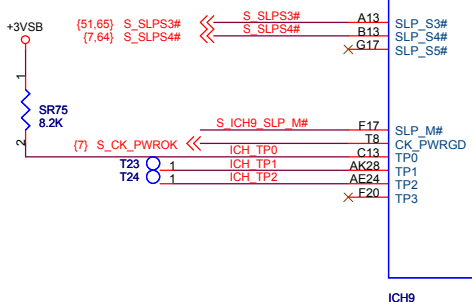
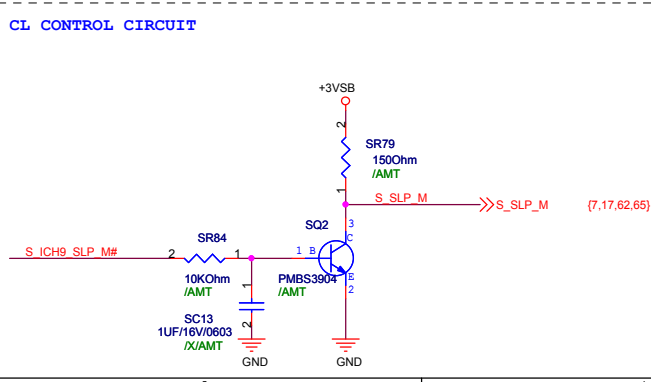
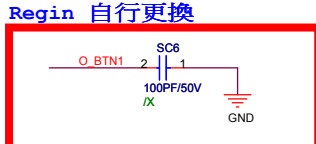
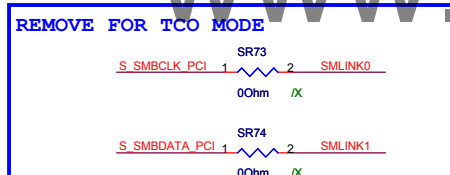
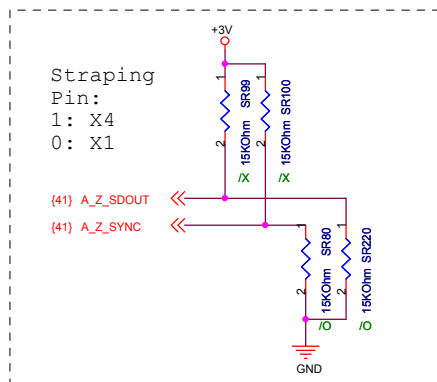
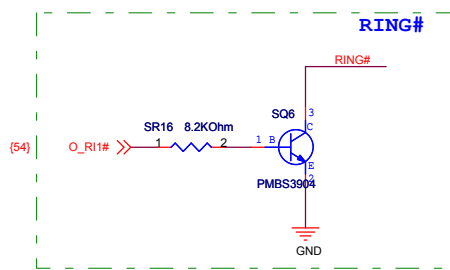
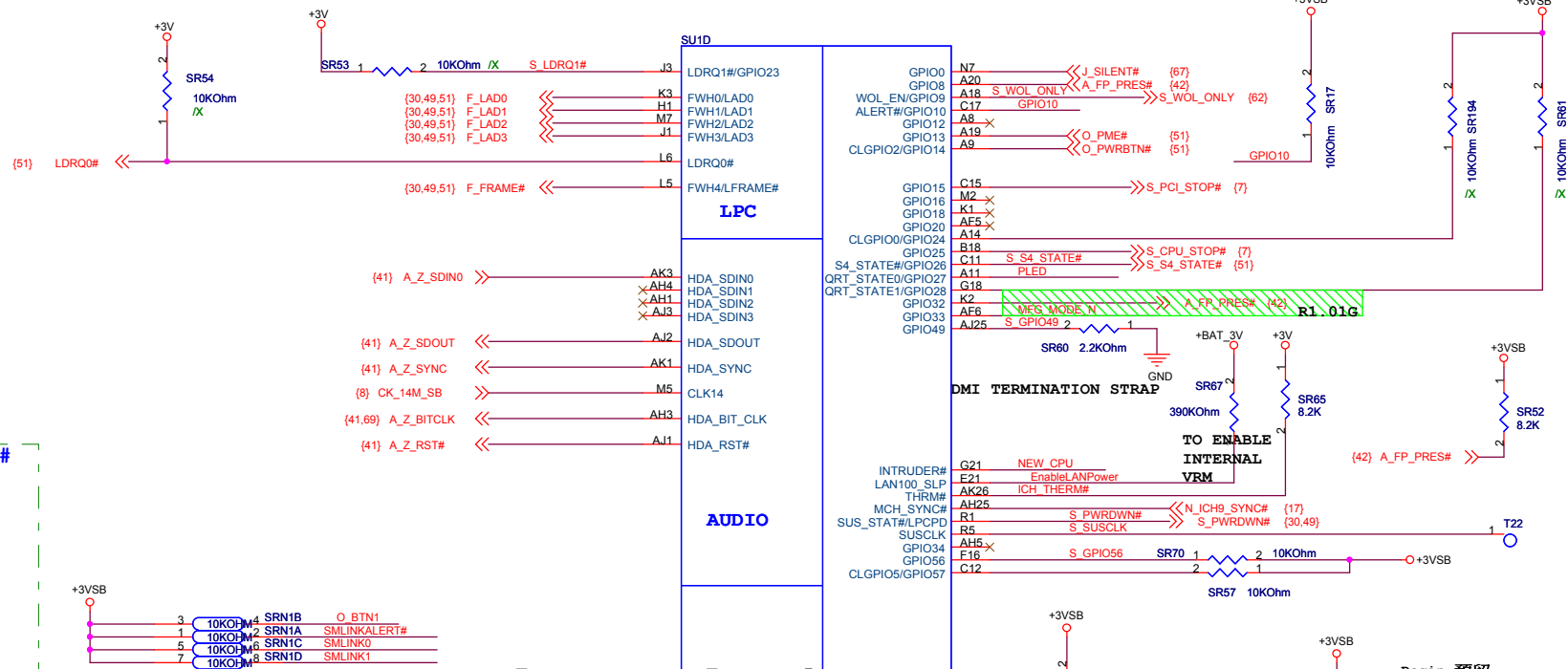


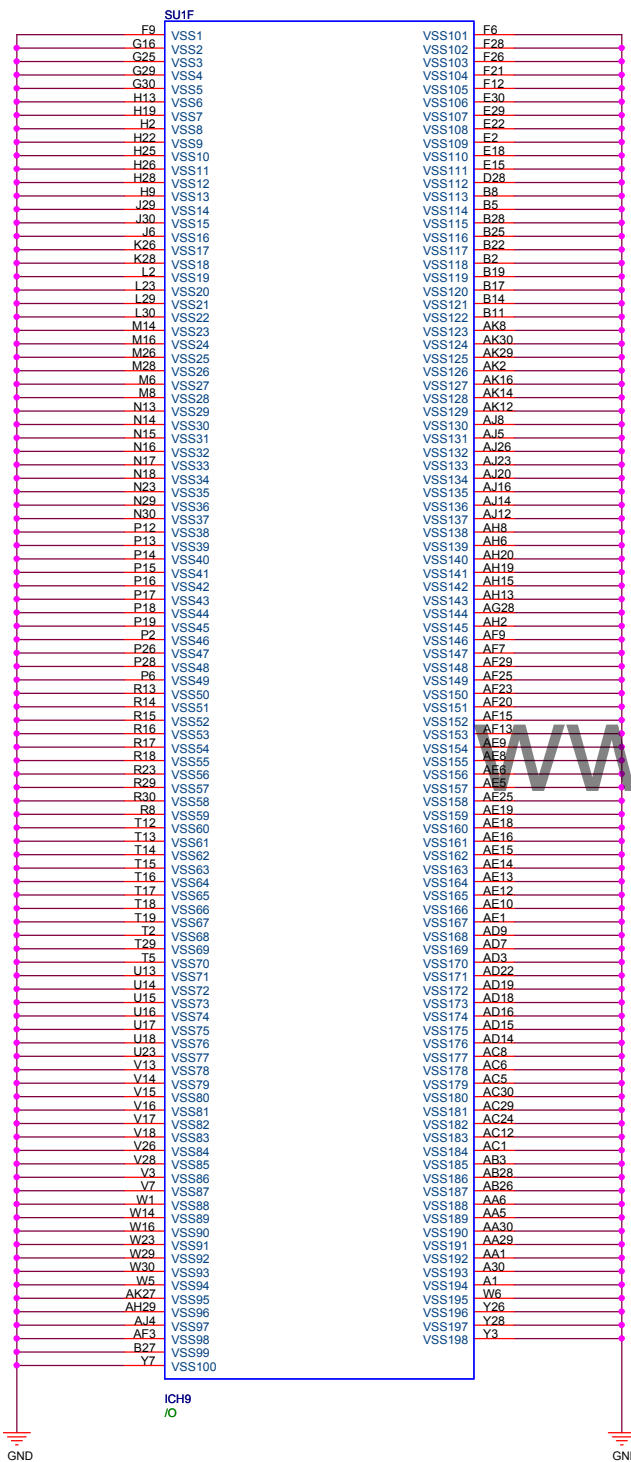
www.aitech1.ru

<Variant Name>

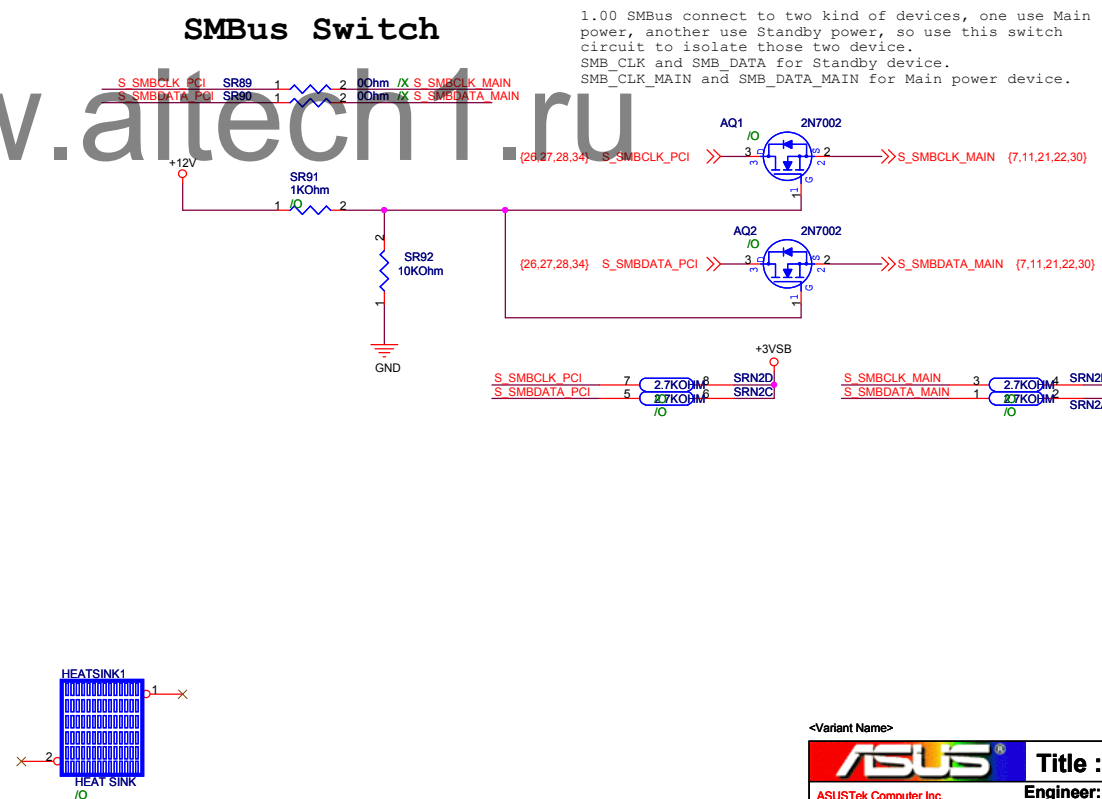
ASUS		Title : ICH9-2	
ASUSTek Computer Inc.		Engineer: Tyler_Yuan	
Size A3	Project Name P5E-VM DO	Rev 1.00G	
Date: Friday, March 28, 2008	Sheet 32	of 70	







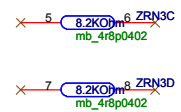
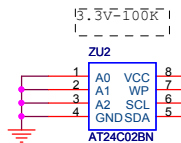
SMBus Switch

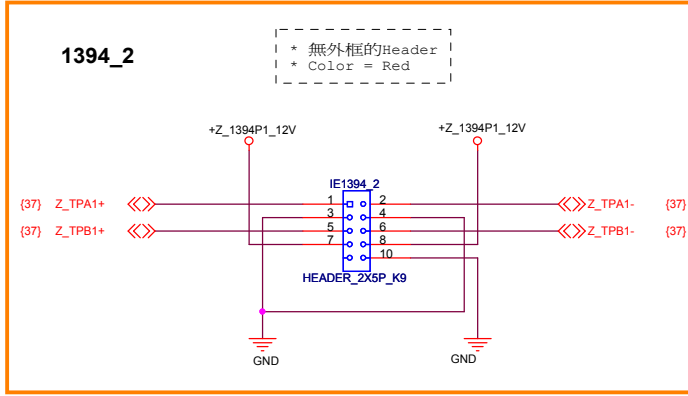


<Variant Name>

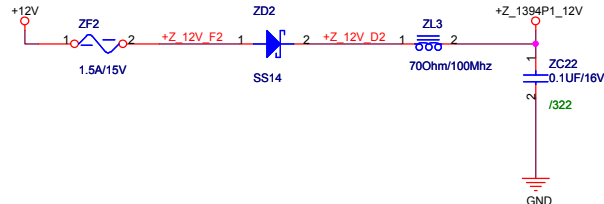
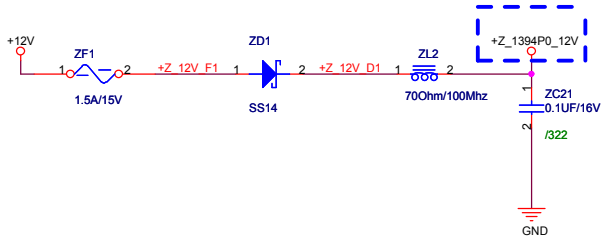
ASUS		Title : ICH9-6	
ASUSTek Computer Inc.		Engineer: Tyler_Yuan	
Size	Project Name	Rev	
A3	P5E-VM DO	1.01G	
Date: Friday, March 28, 2008		Sheet	36 of 70

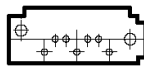
8,31} K_PME#

IX/322

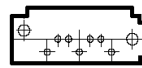


www.aitech1.ru



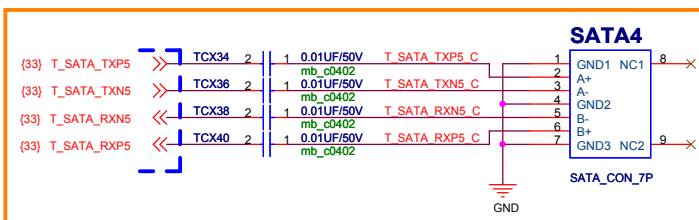
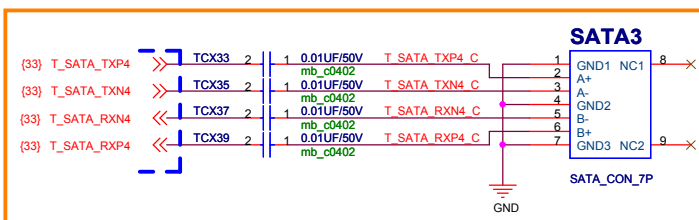
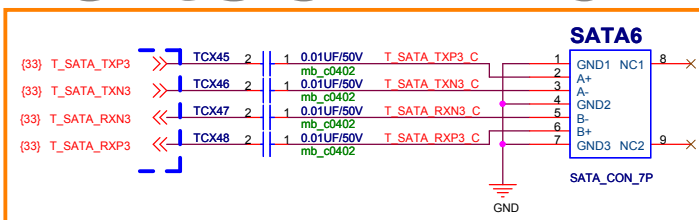
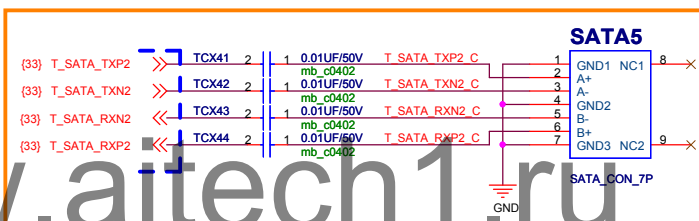
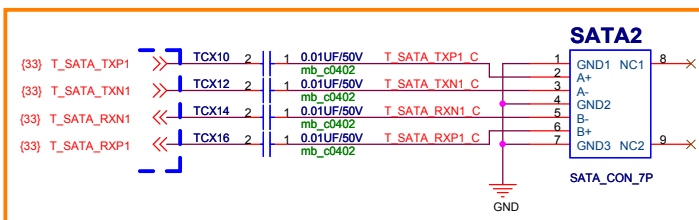
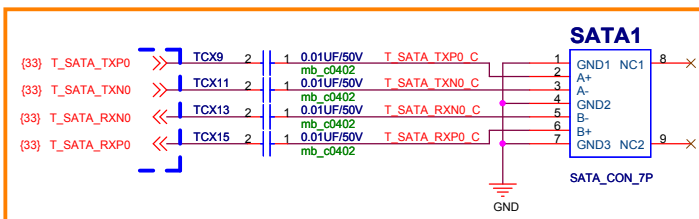


顏色：Black



顏色：RED

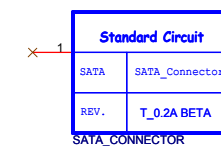
0.2A Beta



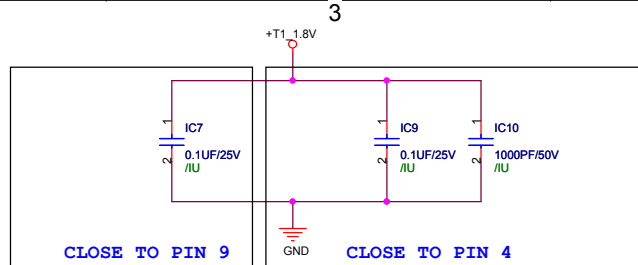
(1) 假如Chipset沒有分Master & Slave, Connector顏色請選擇黑色.

(2) 假如Chipset有分Master & Slave, Master顏色請選擇紅色Connector, Slave顏色請選擇黑色Connector

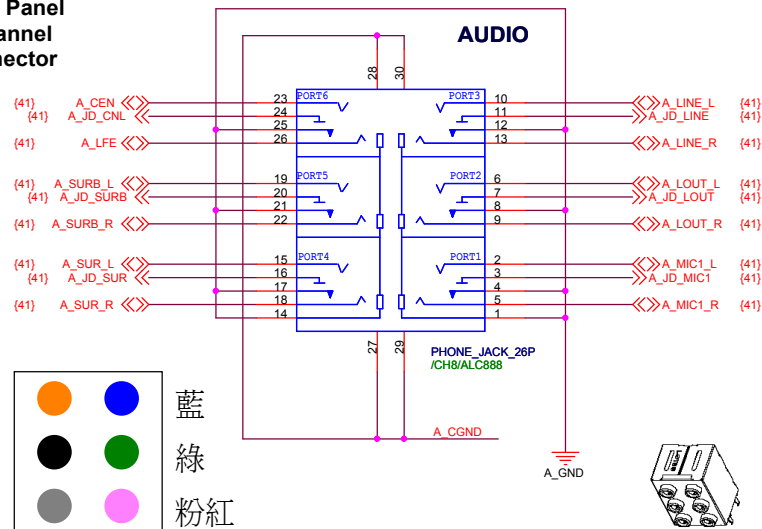
www.aitech1.ru









<Variant Name>


$$V_{out} = V_{ref} * (1 + T1PR2/T1PR1) = 1.25 * (1 + 56.2/120) = 1.835V$$

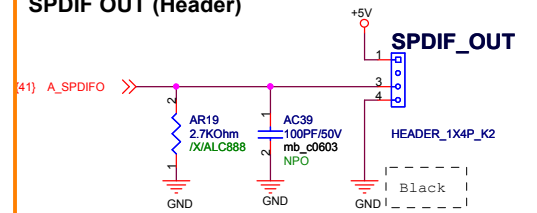
Back Panel 8 Channel Connector



橘			藍
黑			綠
灰			粉紅

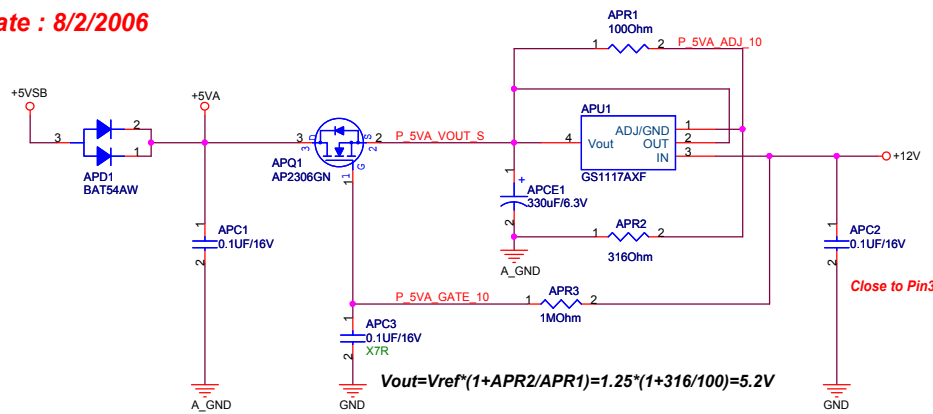
www.aitech1.ru

SPDIF OUT (Header)

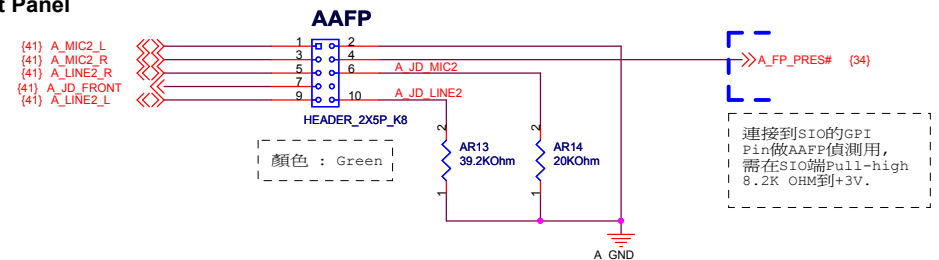


Audio Codec New Solution for Vista !!

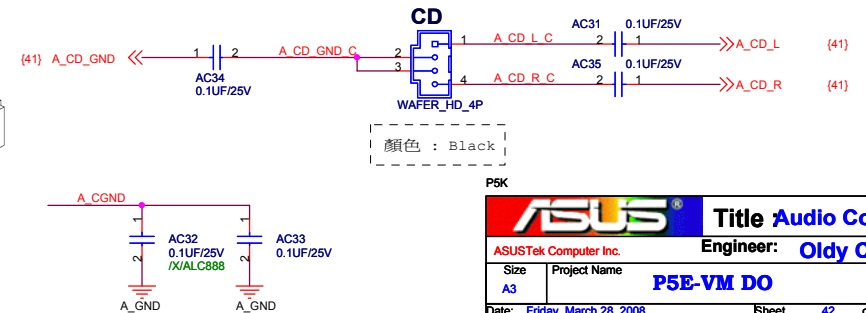
Date : 8/2/2006

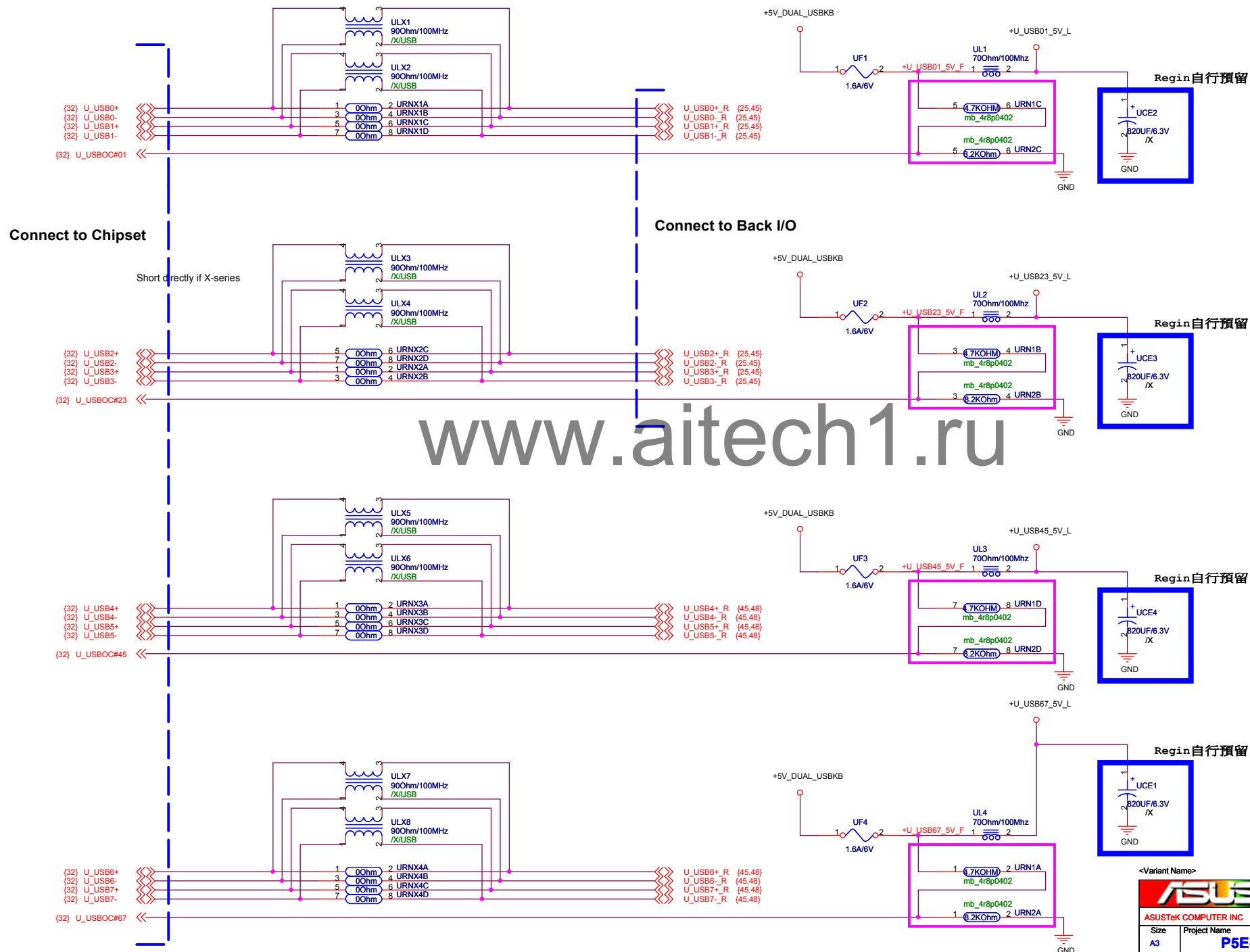


Front Panel

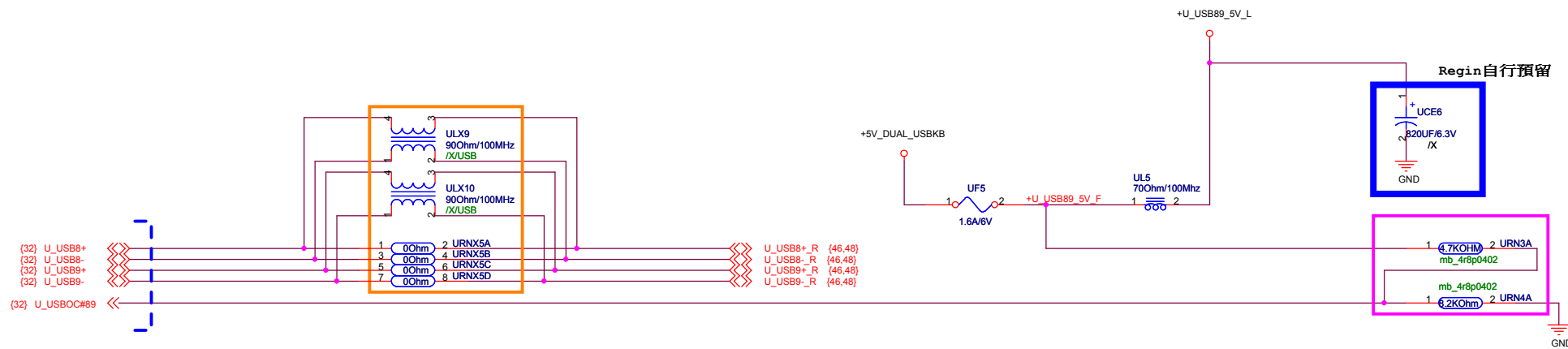


CD IN





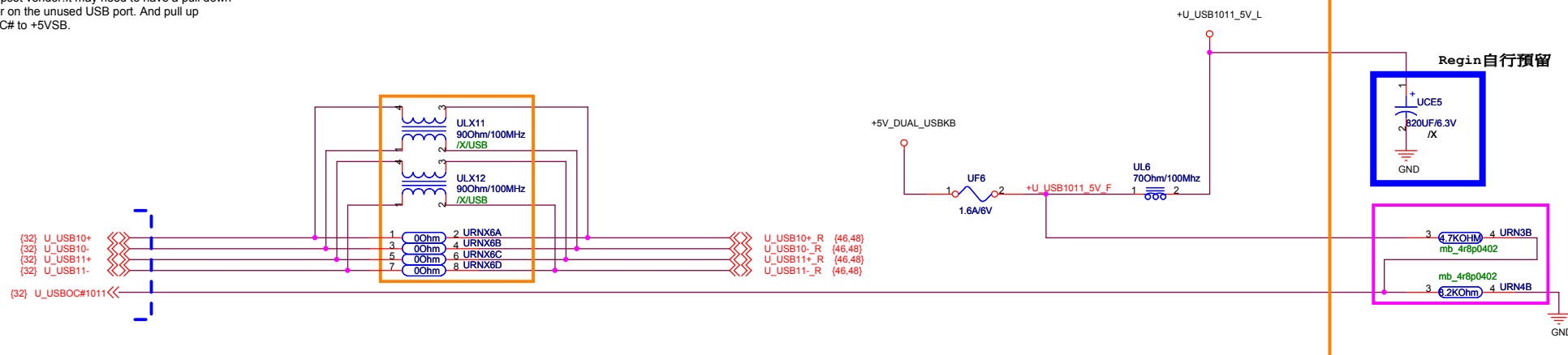
If there are unused USB ports, you need check with the chipset vendor. It may need to have a pull down resistor on the unused USB port. And pull up USB0C# to +5VSB.



C.2

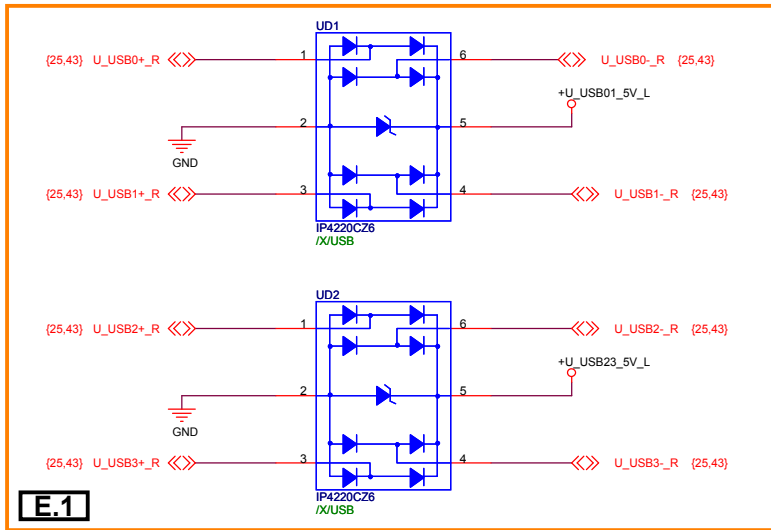
www.aitech1.ru

If there are unused USB ports, you need check with the chipset vendor. It may need to have a pull down resistor on the unused USB port. And pull up USB0C# to +5VSB.



Back I/O USB ESD Protection (IP4220CZ6 or BAV99)
Port 1~4

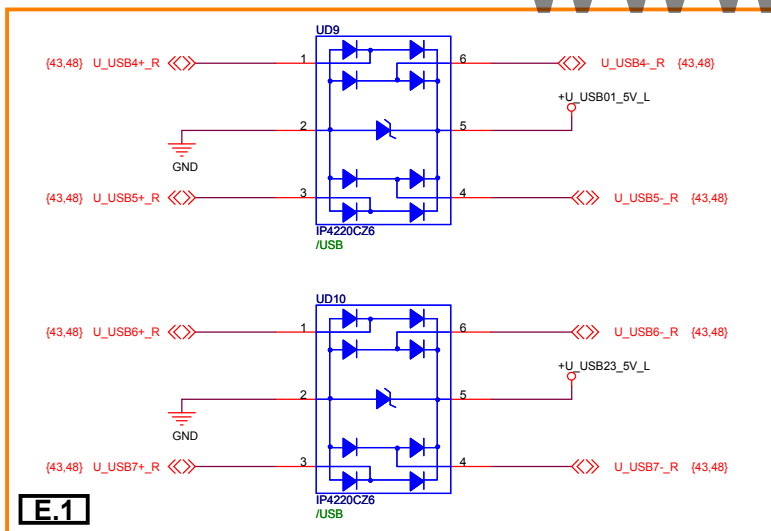
一般使用BAV99，使用IP4220CZ6需主管Review同意



E.1

Back I/O USB ESD Protection (IP4220CZ6 or BAV99)
Port 5~8

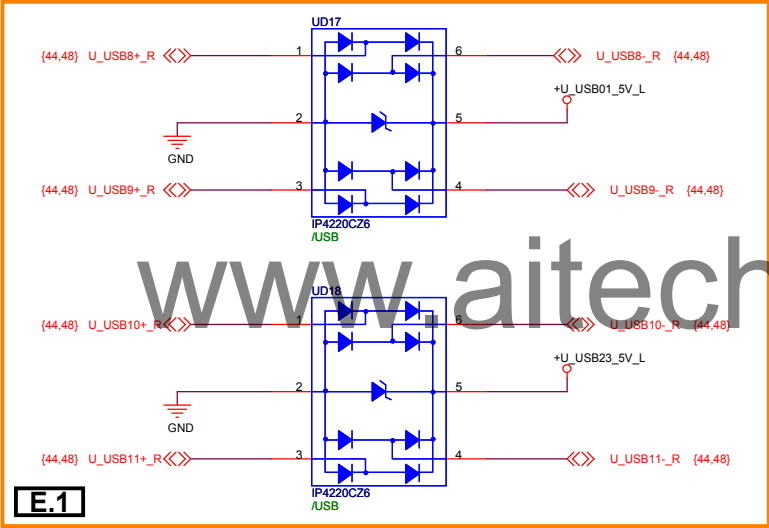
一般使用BAV99，使用IP4220CZ6需主管Review同意



E.1

Back I/O USB ESD Protection (IP4220CZ6 or BAV99)
Port 5-8

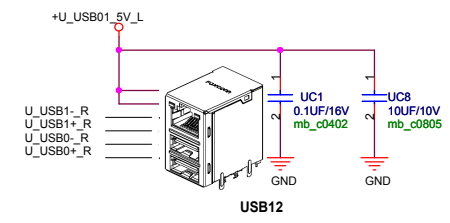
一般使用BAV99，使用IP4220CZ6需主管Review同意



Connect to Back I/O

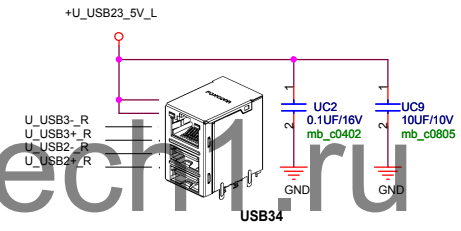
USB12

Choose a proper connector in page "Back I/O Connector"



USB34

Choose a proper connector in page "Back I/O Connector"

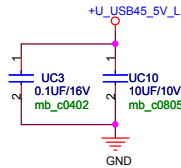
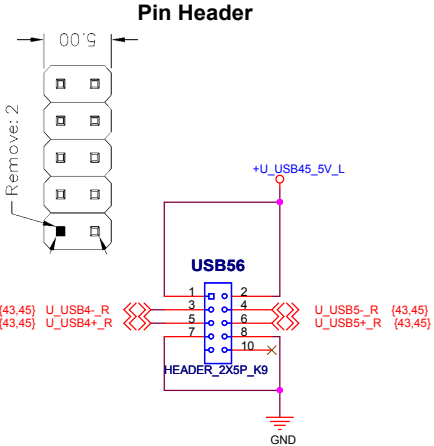


www.aitech1.ru

<Variant Name>

USB56
Internal
Connector

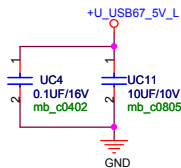
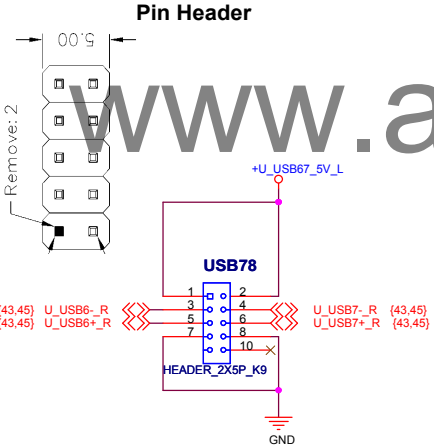
Tow choice:
Box Header or Pin Header



Standard Circuit	
USB+WiFi	USB (ESD) +WiFi (Connector)
REV.	USB 0.2A BETA
USB+WiFi+ASAP //USB	

USB78
Internal
Connector

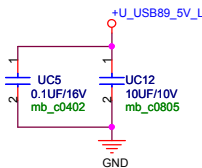
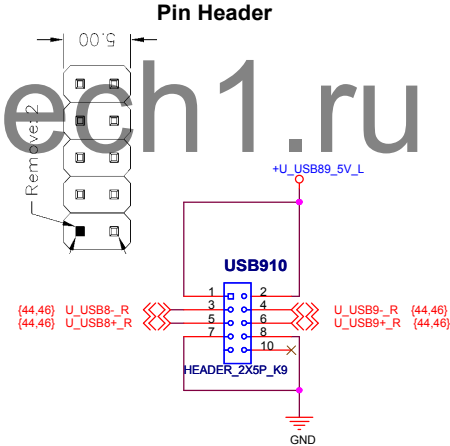
Tow choice:
Box Header or Pin Header



ASAP和WiFi Module頁已經
保留了電容，如果此Port不
上Box Header (Pin Header)
而上ASAP或WiFi Module
，可以連電容
一起刪掉

USB910
Internal
Connector

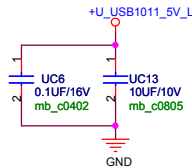
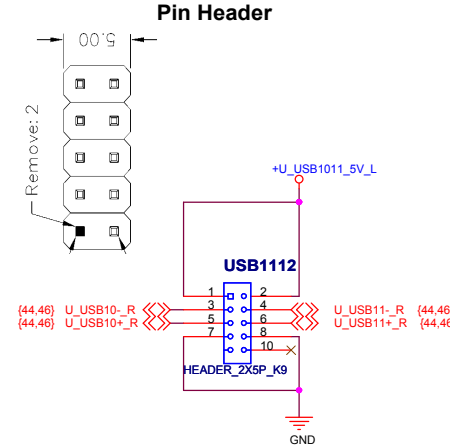
Tow choice:
Box Header or Pin Header



ASAP和WiFi Module頁已經
保留了電容，如果此Port不
上Box Header (Pin Header)
而上ASAP或WiFi Module
，可以連電容
一起刪掉

USB1112
Internal
Connector

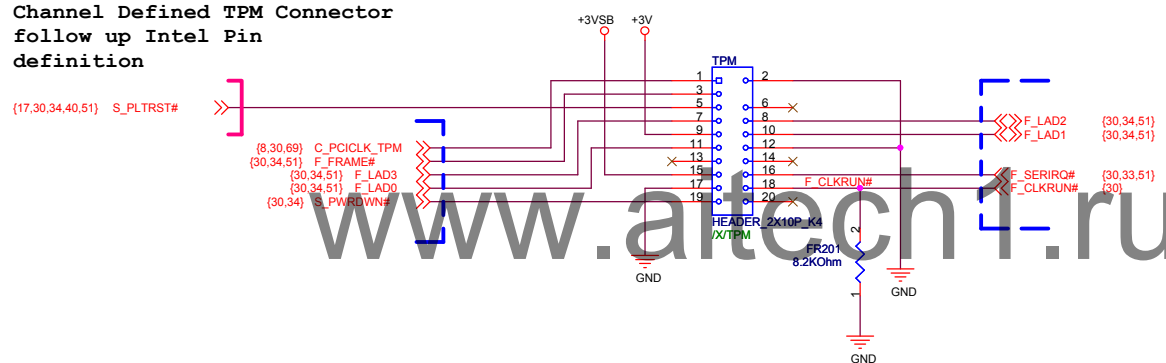
Tow choice:
Box Header or Pin Header



ASAP和WiFi Module頁已經
保留了電容，如果此Port不
上Box Header (Pin Header)
而上ASAP或WiFi Module
，可以連電容
一起刪掉

<Variant Name>		Title : USB_Port3~12(Int.)	
ASUSTek COMPUTER INC		Engineer: Nick Kao	
Size A3	Project Name P5E-VM DO	Rev 0.2A	
Date: Friday, March 28, 2008		Sheet 48 of 70	

Channel Defined TPM Connector
follow up Intel Pin
definition



Standard Circuit	
TPM	TPM_Connector
REV.	F_0.1B BETA

TPM CONNECTOR /X/TPM

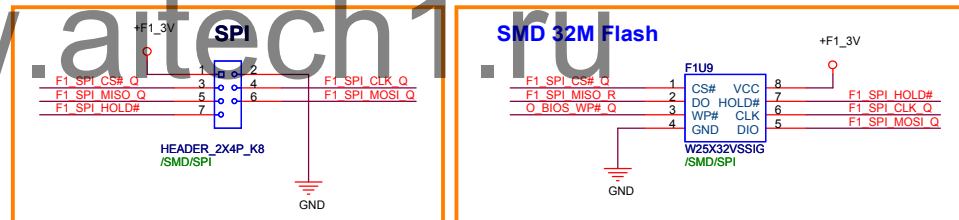
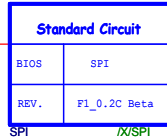
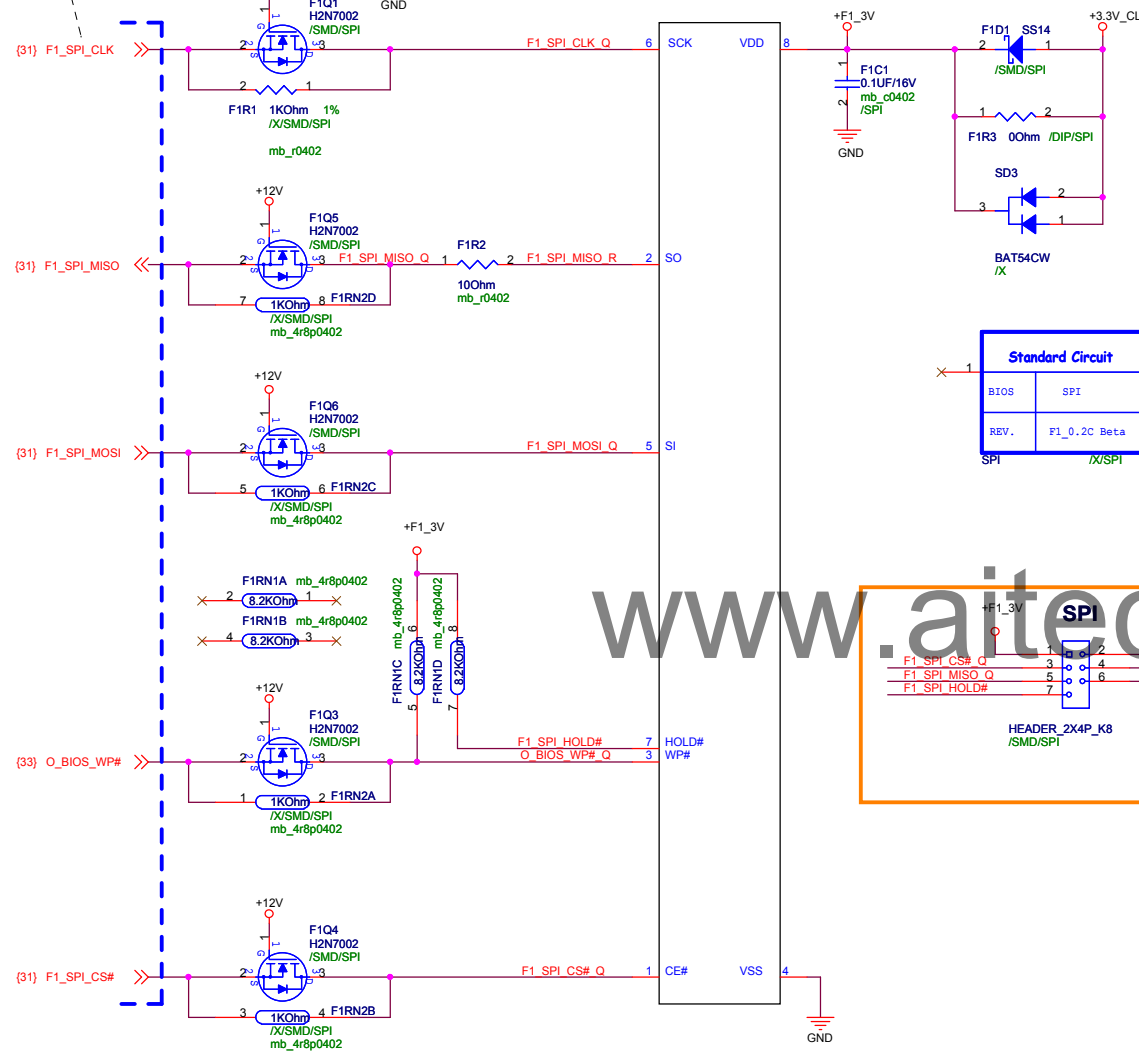
F1_SPI_CLK
F1_SPI_MOSI
F1_SPI_CS#

等net須在SB端留
series termination resistor

F1C2

擺靠近F1Q1, F1Q5, F1Q6附近,
避免+12V的noise couple到F1_SPI_CLK,
F1_SPI_MOSI, F1_SPI_MISO等訊號

選擇BOM要上的Flash, 其餘請刪除。



SPI SMD 4M Flash P/N

Priority 1
SST : 05G00100H210
Priority 2
PMC : 05G001015311
Priority 3
ATMEL : 05G00100L010
Priority 4
Winbond : 05G00100F130

SPI SMD 8M Flash P/N

Priority 1
ST : 05G001208031
Priority 2
SST : 05G00120A010
Priority 3
MXIC : 05G001217012
Priority 4
Winbond : 05G001208130
Priority 5
ATMEL : 05G00120B010

SPI SMD 16M Flash P/N

Priority 1
SST : 05G001405010
Priority 2
MXIC : 05G001403010
Priority 3
ST : 05G001418020
Priority 4
ATMEL : 05G001409010
Priority 5
SPANSION : 05G001405111

SPI SMD 32M Flash P/N

Priority 1
Winbond : 05G00160D110

DIP & SMD SPI FLASH CO-LAYOUT BOM OPTIONAL :

DIP SPI FLASH BOM OPTIONAL :

選擇 /DIP/SPI & /X/SPI & /SPI

SMD SPI FLASH BOM OPTIONAL :

選擇/X/SMD/SPI & /SMD/SPI
/X/SPI & /SPI

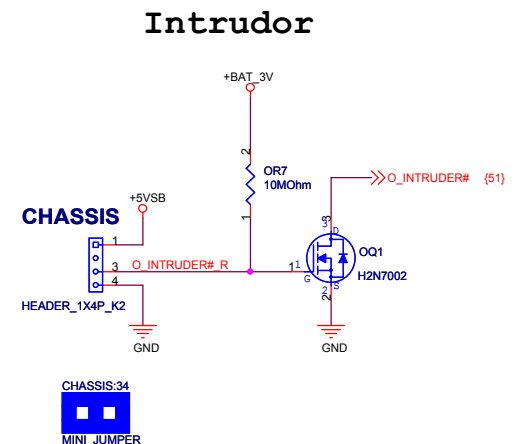
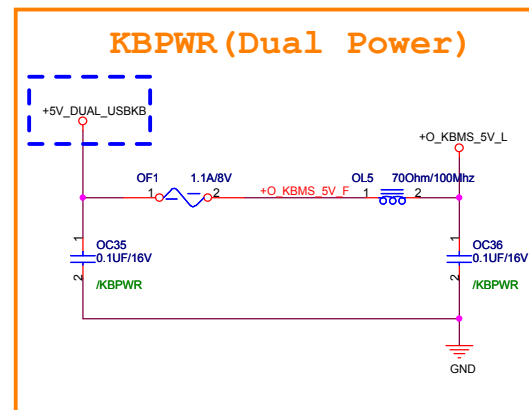
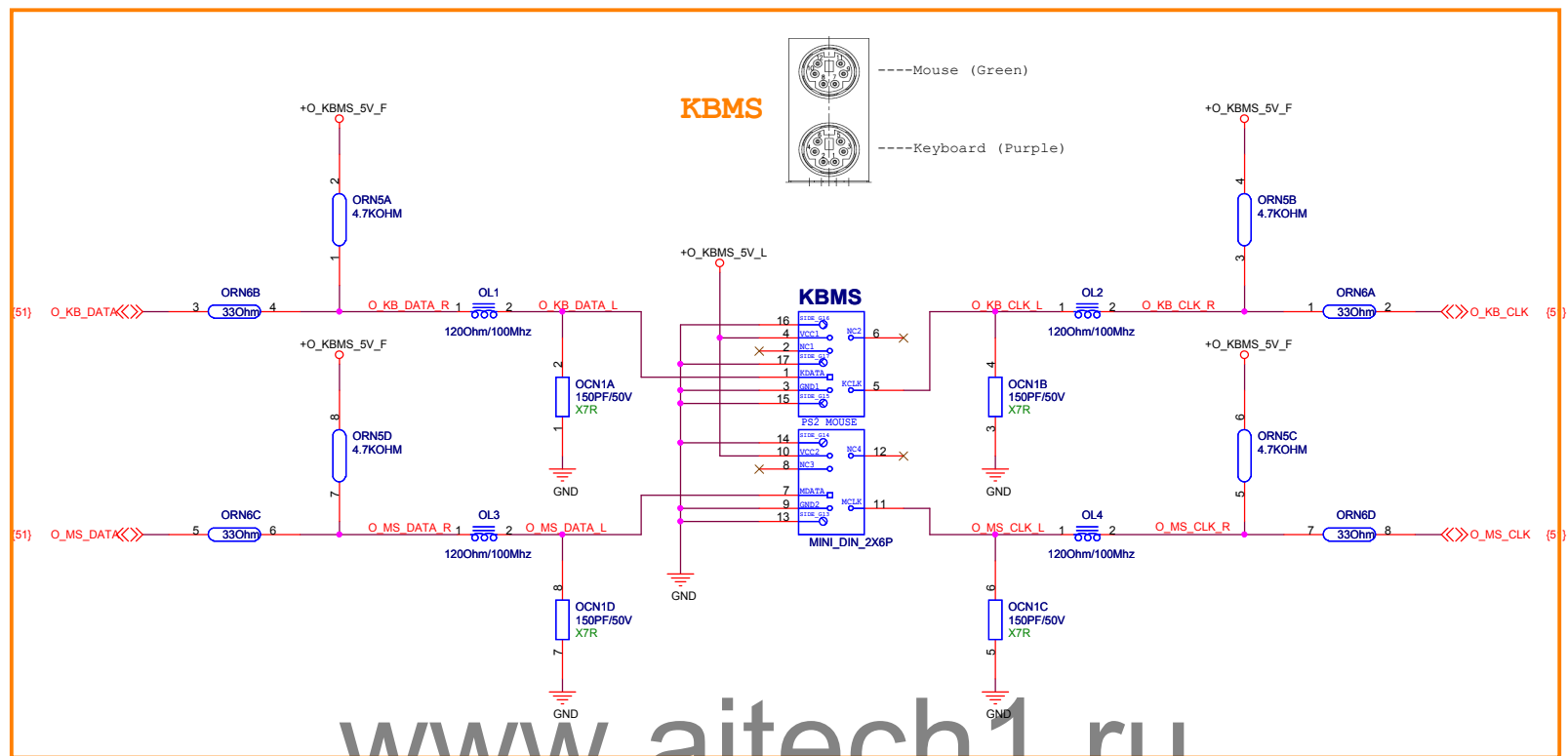
F1Q1, F1Q5, F1Q6, F1Q3, F1Q4,
F1C2, SPI, F1D1
BOM Optional選擇不上。

F1R1N2及F1R1請RD手動改上0 ohm
F1R1N2 : 10V253000040
F1R1 : 10V213000040

<Variant Name>

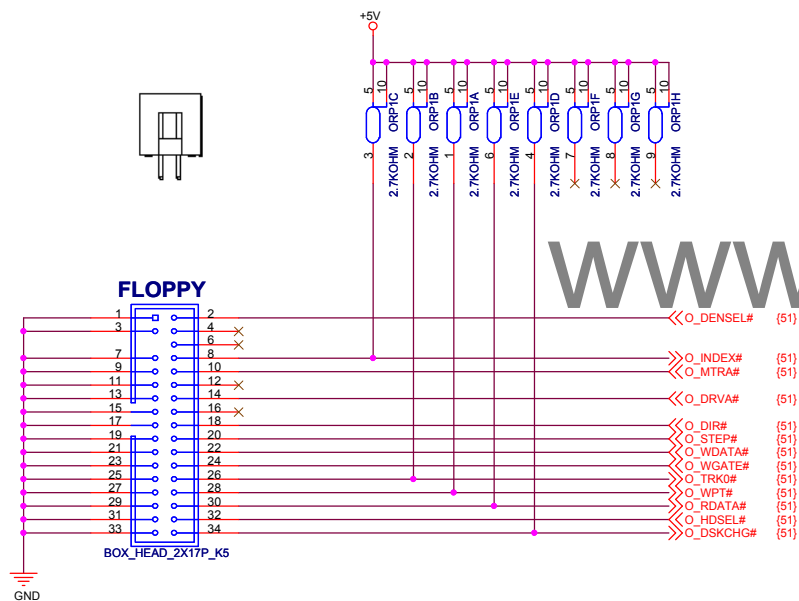
ASUS		Title : SPI	
ASUSTek Computer Inc.		Engineer: Eddie Chiu	
Size A3	Project Name P5E-VM DO	Rev 0.2C	
Date: Friday, March 28, 2008		Sheet 50 of 70	





<Variant Name>

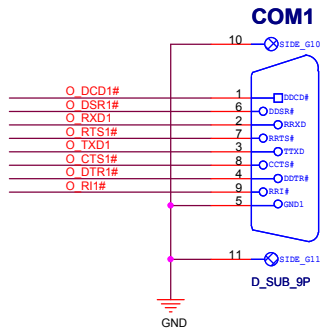
Floppy, Standard (Default)



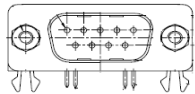
www.aitech1.ru

<Variant Name>

COM1 Right Angle (Default)

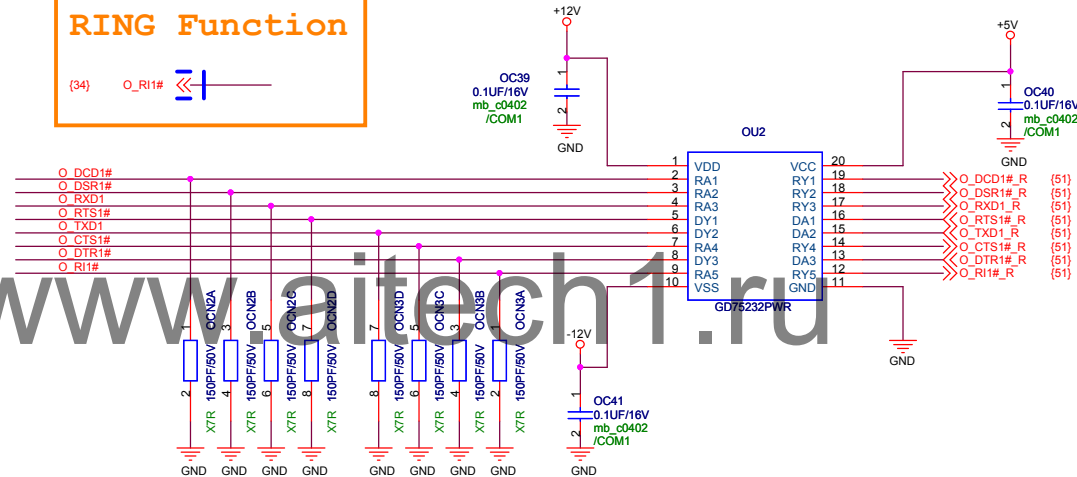


(Green)
(Standard)



RING Function

(34) O_RI1#

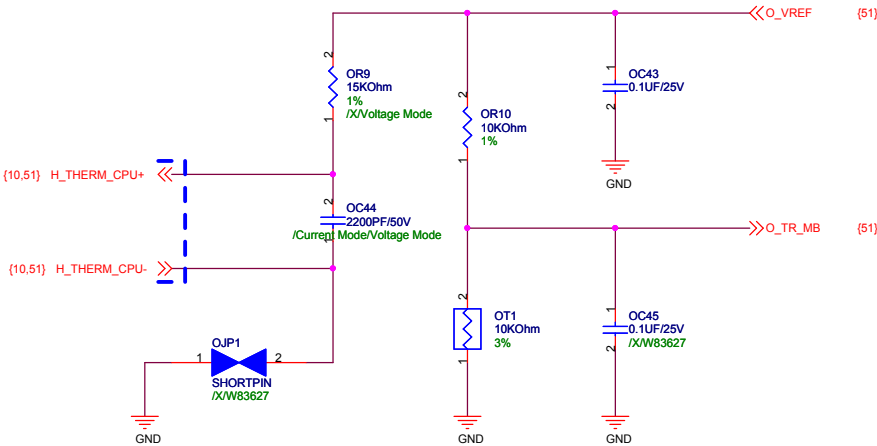


<Variant Name>

Hardware Monitor for Temperature

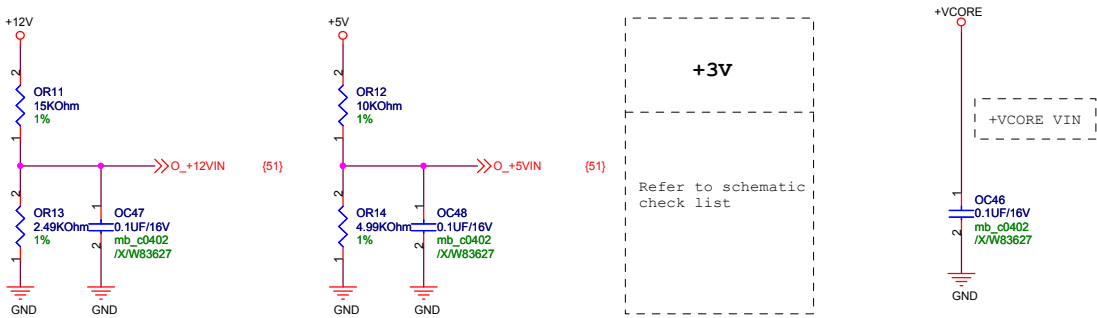
BOM Option

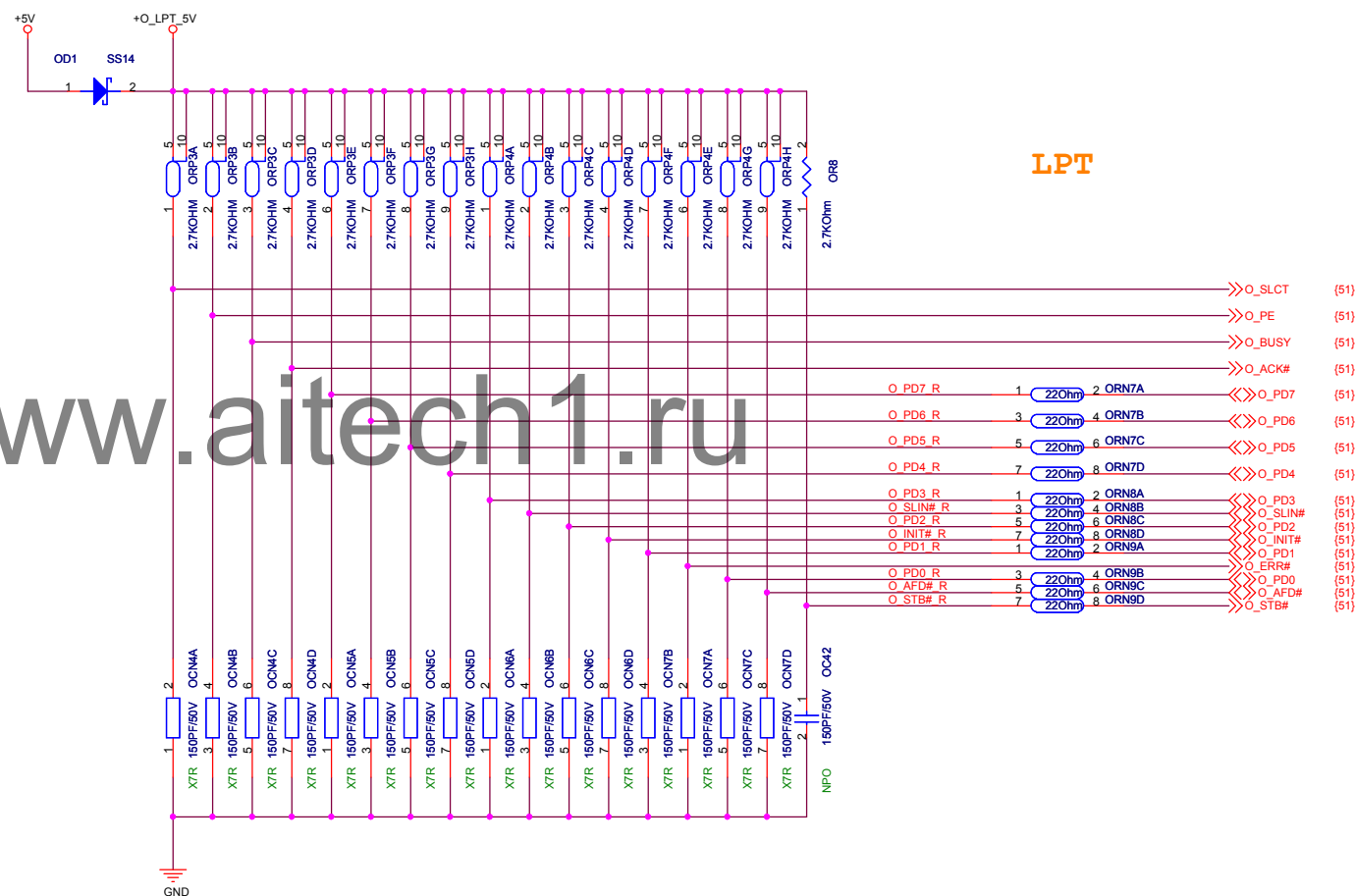
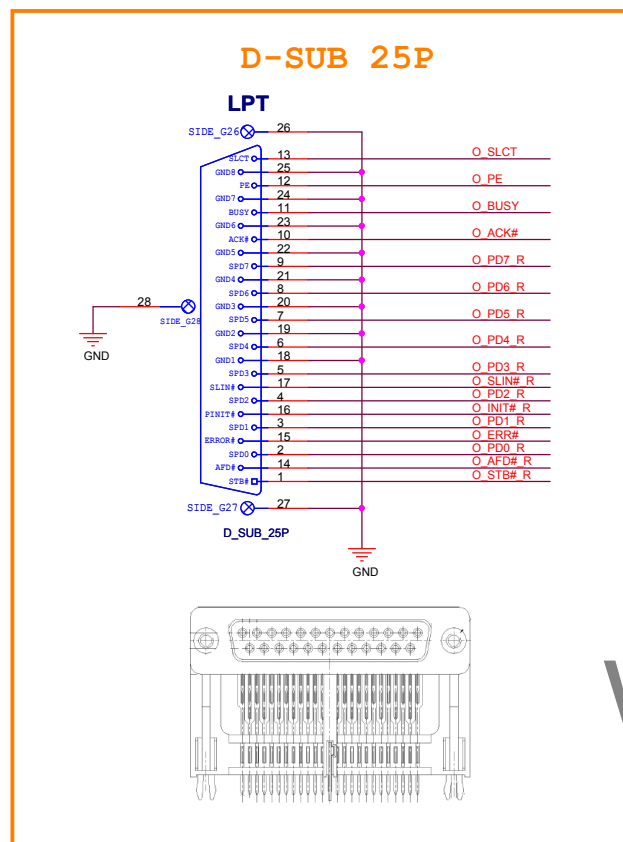
	Voltage Mode	Current Mode (Default)
OR9	V	X
OC44	V	V



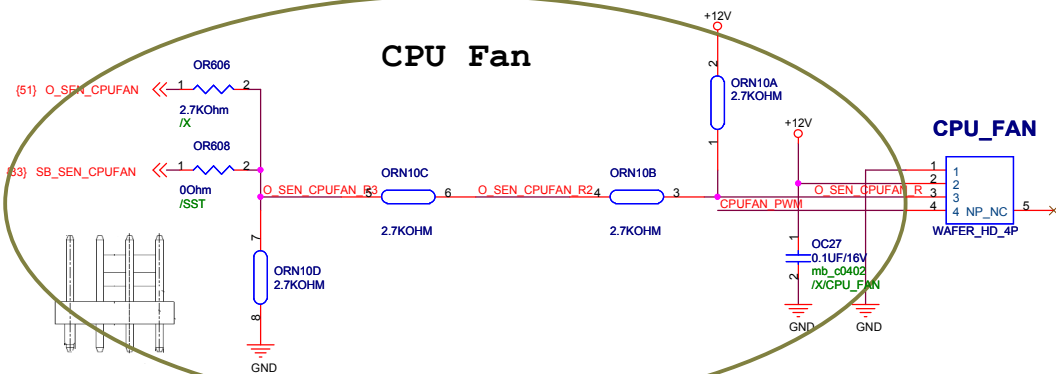
www.aitech1.ru

Hardware Monitor for VIN

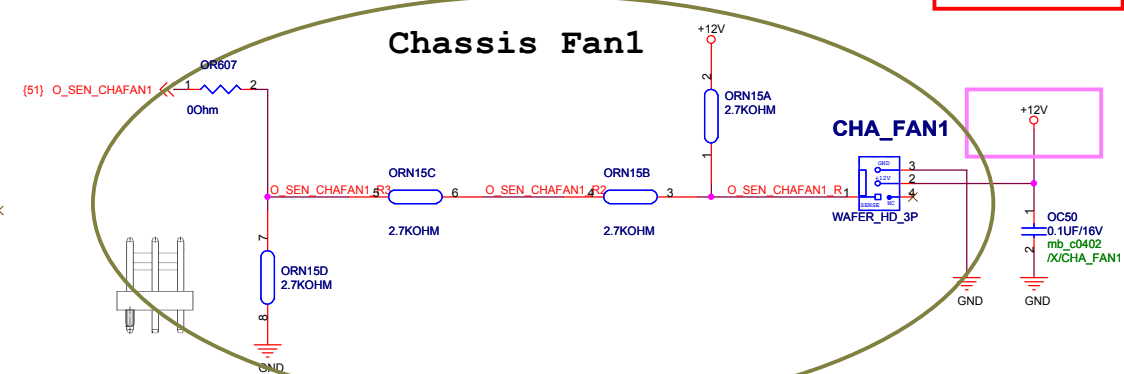




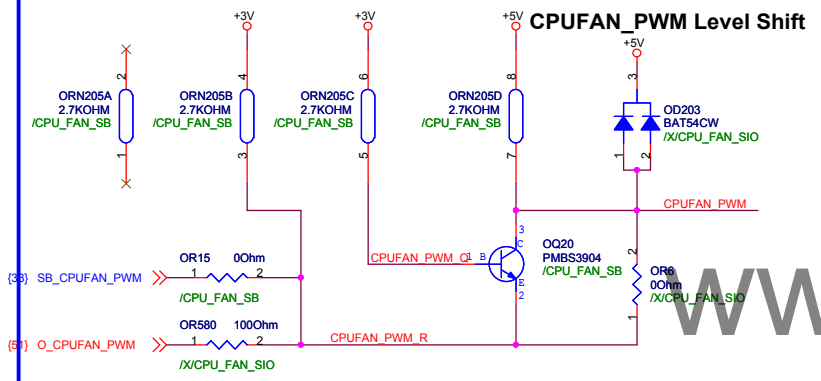
CPU Fan



Chassis Fan1



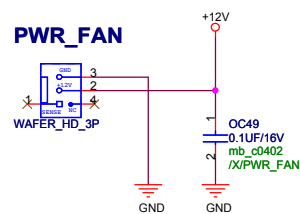
CPUFAN_PWM Level Shift



DEL
ORN11
20070125

Power Fan

PWR_FAN

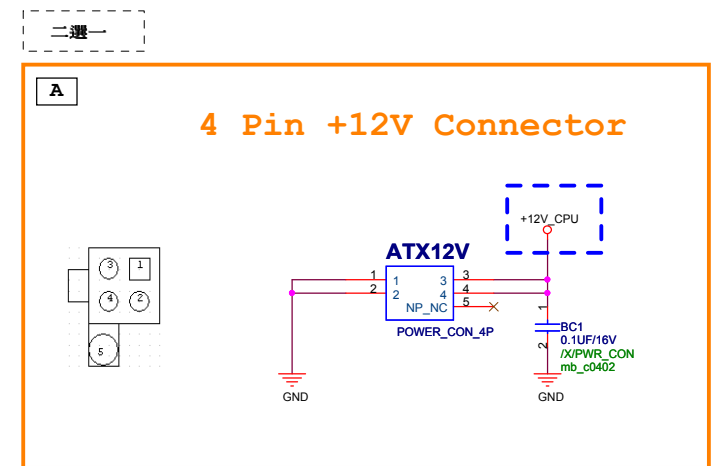
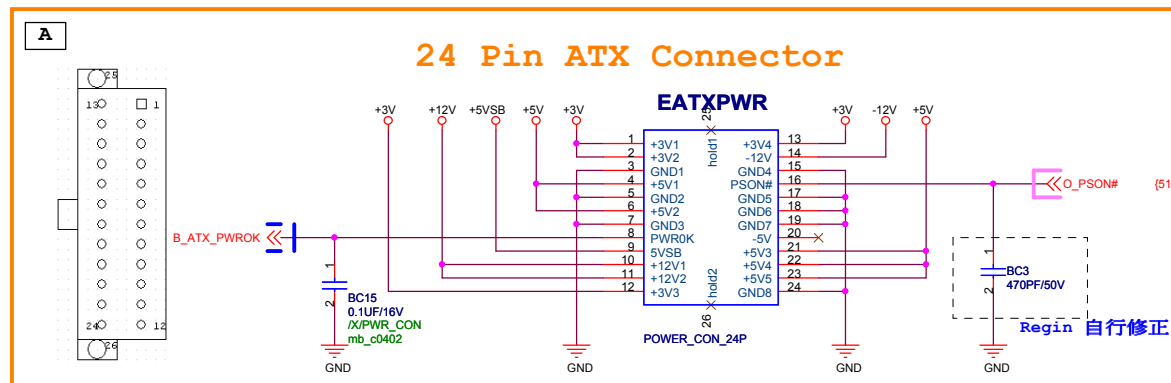


www.aitech1.ru

CPU_FAN BOM Option

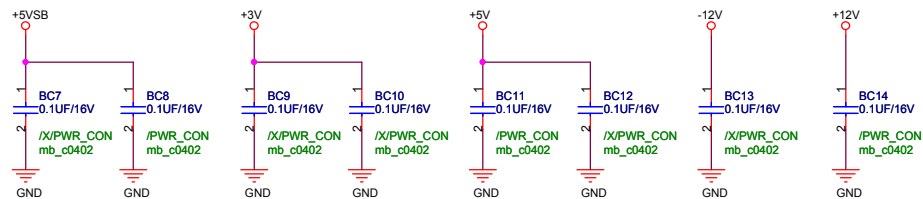
	SB Control /CPU_FAN_SB	SIO Control /CPU_FAN_SIO
OR580	X	V
OR6	X	V
OD203	X	V
OR15	V	X
ORN205	V	X
OQ20	V	X

<Variant Name>



www.aitech1.ru

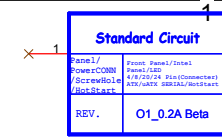
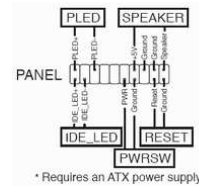
Bypass/EMI Capacitor



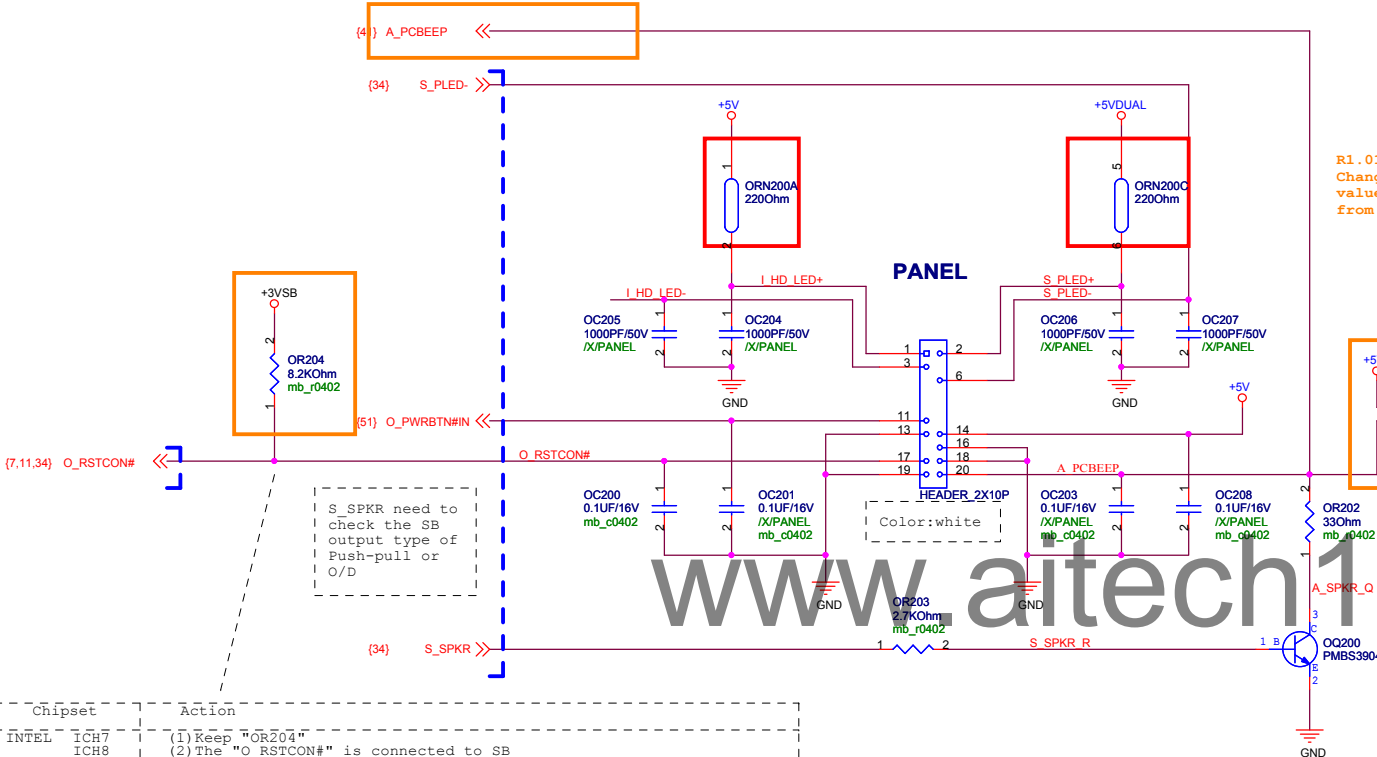
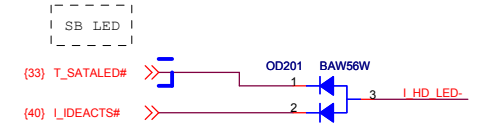
Front Panel

PART Reference 與SIO共用0 並從200編起

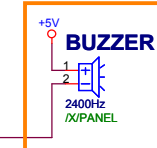
```
Can be del if you  
don't connect to  
AUDIO
```



HD_LED



```
R1.01G:Regin
Change ORN200 STD circuit
value
from 300 ohm to 220 ohm
```

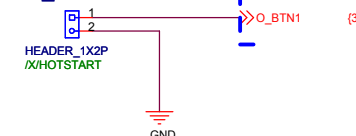


```
| Change the net name to combine the HD LED active |
| 請按照下列 Net name 修改: I_IDEACTP#          |
|                                     II_IDEACTP#      |
|                                     I_IDEACTS#       |
|                                     II_IDEACTS#       |
|                                     T1_SATALED#      |
|                                     T2_SATALED#      |
| 用不到的 net 請Delete,並打x                    |
```

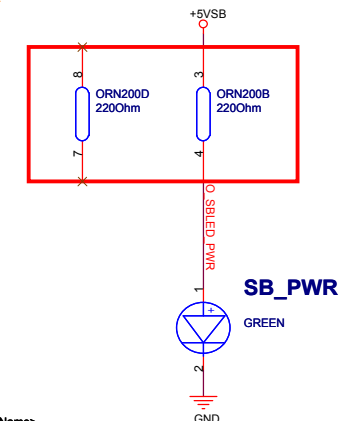
Chipset	Action
INTEL ICH7 ICH8 ICH9	(1)Keep "OR204" (2)The "O_RSTCON#" is connected to SB (3)Delete "O_RSTCON#" off-page net on SIO page
Nvidia CK804 MCP51	(1)Keep "OR204" (2)The "O_RSTCON#" is connected to SB (3)Delete "O_RSTCON#" off-page net on SIO page (4)add serial R (22 ohm) on "O_RSTCON#" by AP note for ESD issue,please add R on chipset page.
VIa VT8237 VT8251	(1)Delete "OR204" (2)The "O_RSTCON#" is connected to SIO (3)Check pull-up resistor & pull-up level on SIO page
SIS 965L	(1)Delete "OR204" (2)The "O_RSTCON#" is connected to SIO (3)Check pull-up resistor & pull-up level on SIO page
ATI SB600	(1)Delete "OR204" (2)The "O_RSTCON#" is connected to SIO (3)Check pull-up resistor & pull-up level on SIO page

二選一 需確認 PES 或與 PM 確認

Hot Start



Standby LED



<Variant Name>



Title : Panel&HotStart

ASUS TeK Computer INC

Engineer: Kenny Chen

Size	Project Name
------	--------------

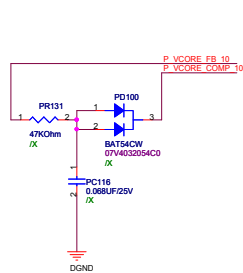
P5E-VM DO

Rev

Date: Friday, March 28, 2008

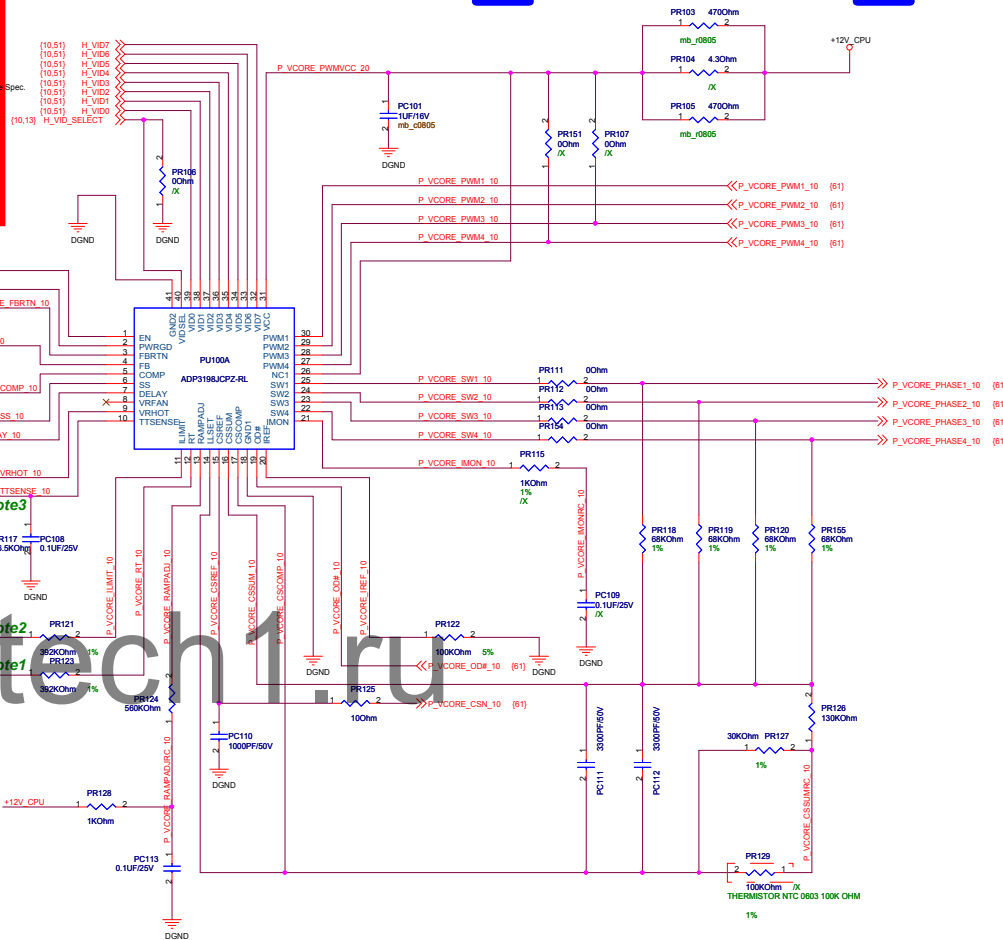
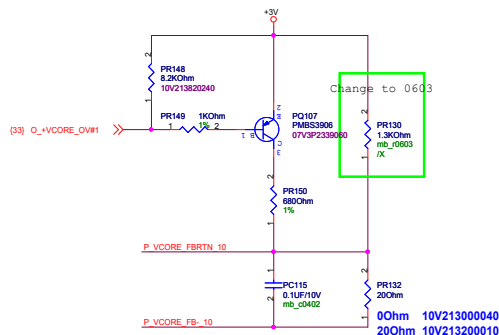
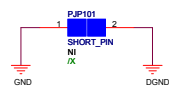
Sheet 59 of 70

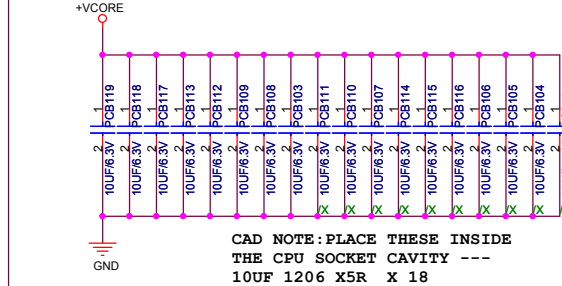
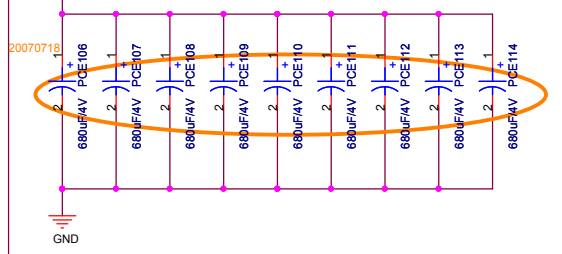
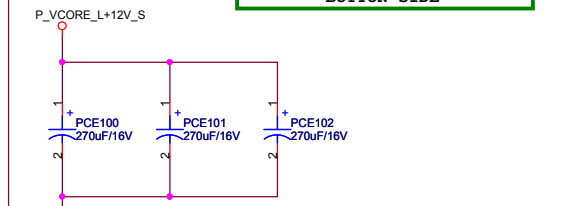
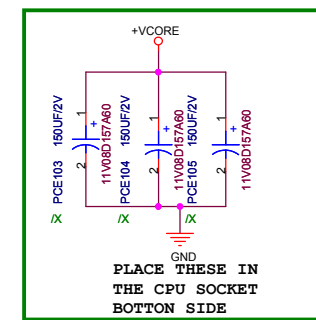
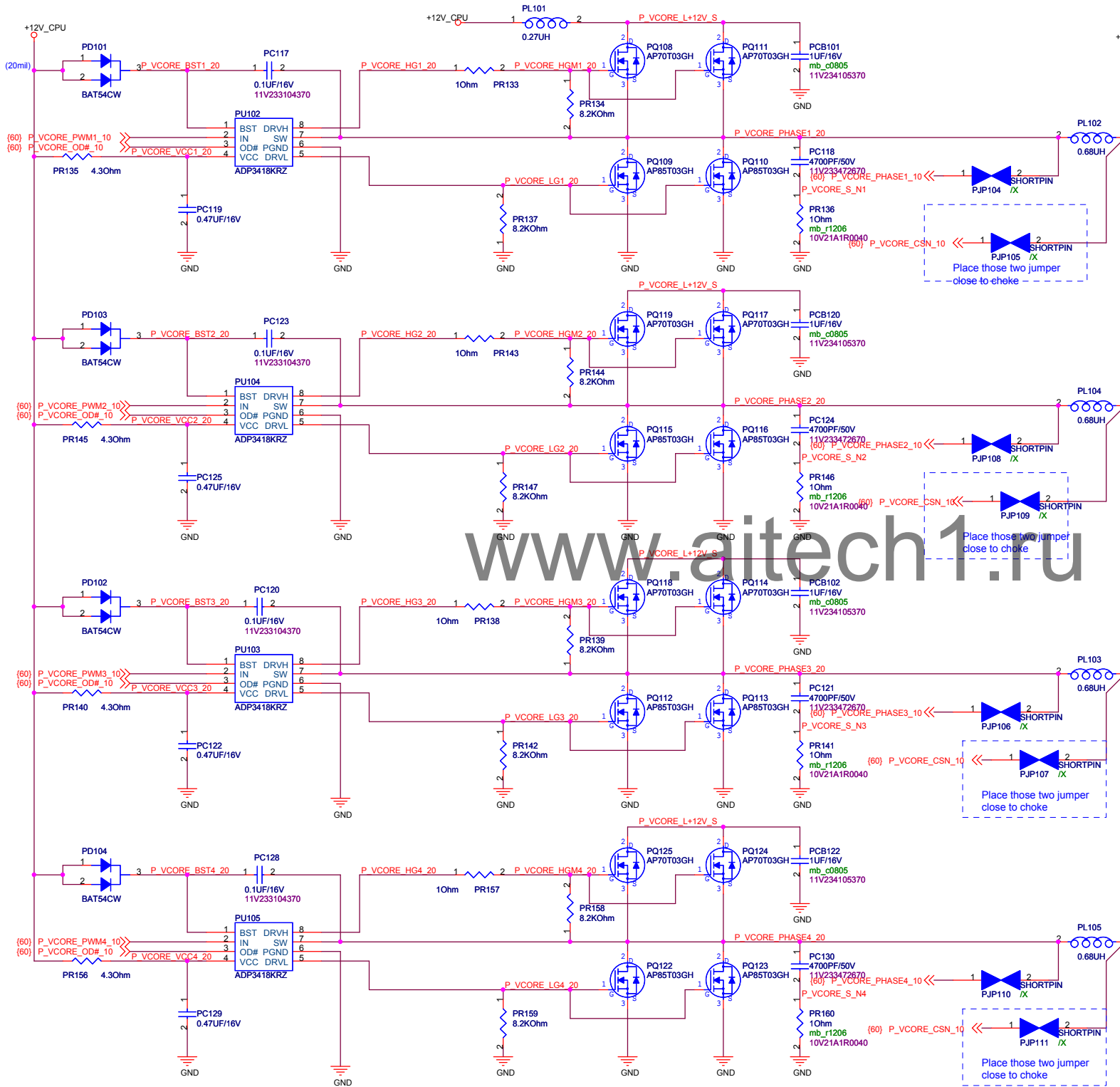
The schematic diagram illustrates the power management section of the PMS33904, specifically the connection of the P_VRM_GD pin to the P_VTT_PWRGD pin. The circuit is powered by a +3V supply and includes a 2KOhm resistor (PRN101A) and a 560Ohm resistor (PR102). The P_VRM_GD pin is connected to the P_VTT_PWRGD pin via a network of resistors and capacitors. The circuit includes a 3V supply, a 2KOhm resistor (PRN101A), a 560Ohm resistor (PR102), and several capacitors (PMBS3904, PMS33904, PRN101C, PRN101D, PRN101B). The P_VRM_GD pin is connected to the P_VTT_PWRGD pin via a network of resistors and capacitors.



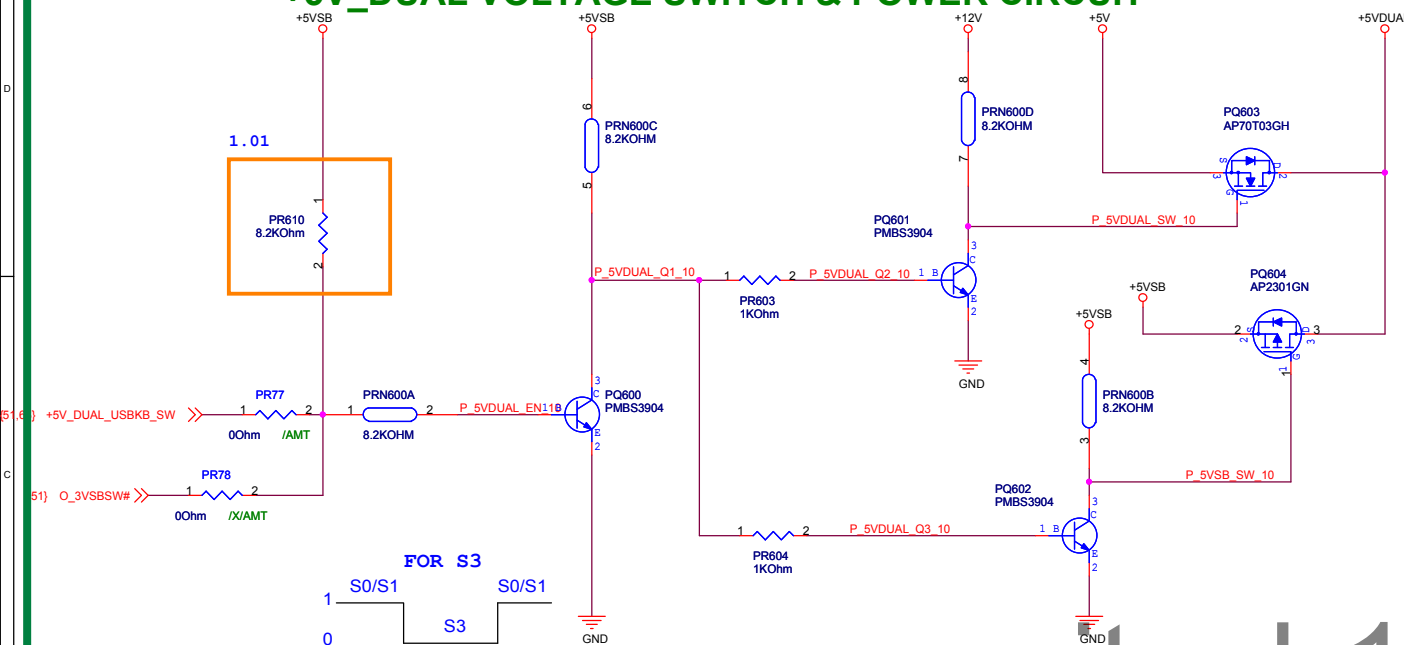
Note6

The diagram shows two PNP transistors, PJP102 and PJP103, used as current sources. PJP102's emitter is connected to +VCCORE (pin 9) and its base to P*VCCORE_FB = 10. Its collector is connected to the collector of PJP103 and to pin 2. PJP103's emitter is connected to GND and its base to P*VCCORE_FB = 10. Its collector is connected to pin 2. A capacitor PC14 (1000PF/50V) is connected between pin 1 and the common collector node (pin 2).

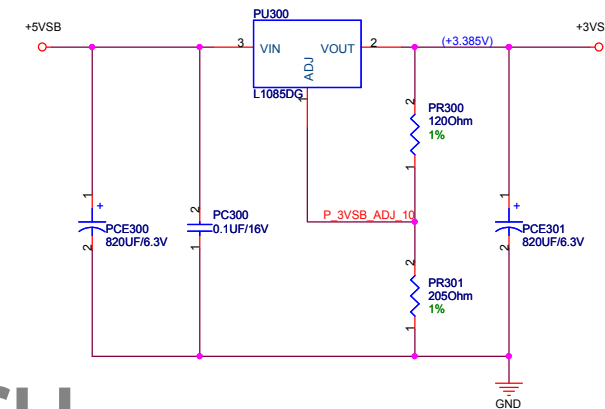




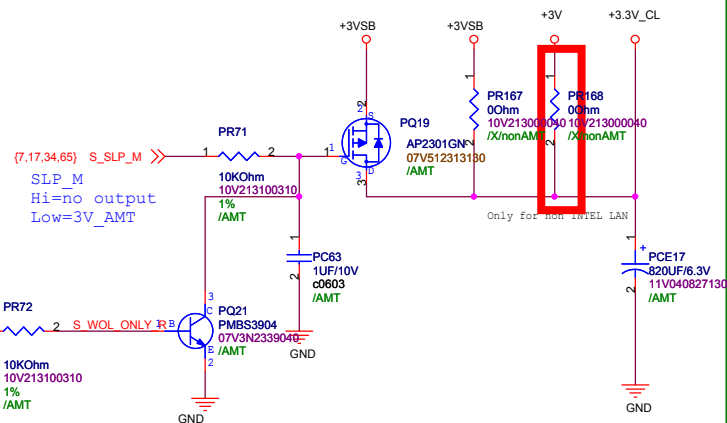
+5V_DUAL VOLTAGE SWITCH & POWER CIRCUIT



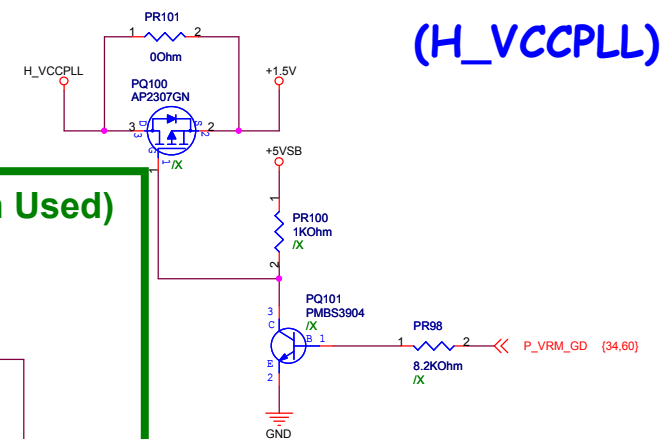
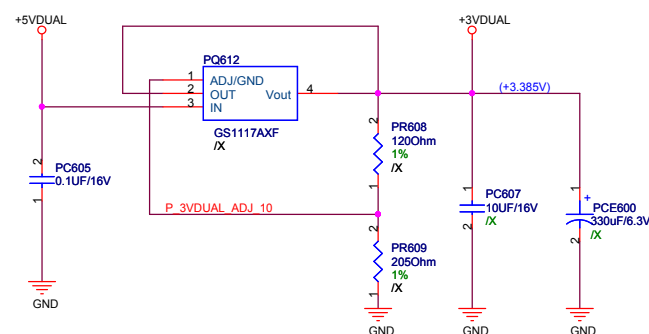
+5VSB ==>+3VSB Io: 2A



+3VSB ==>+3V_CL



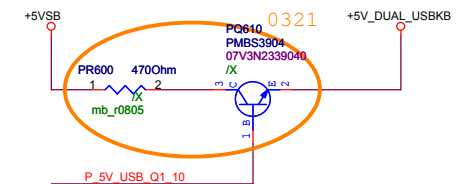
+5VDUAL==>+3VDUAL(Clock Gen Used)

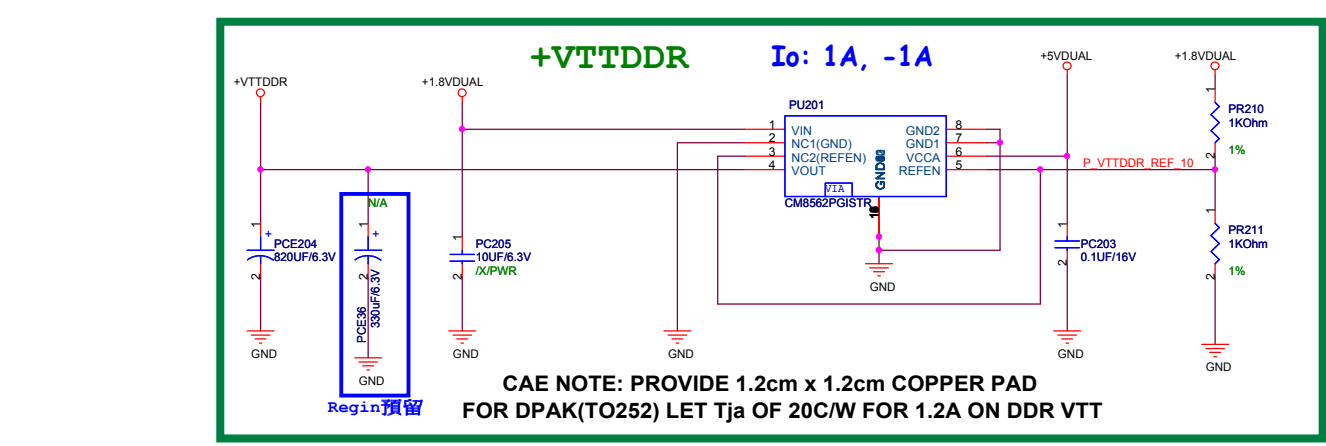
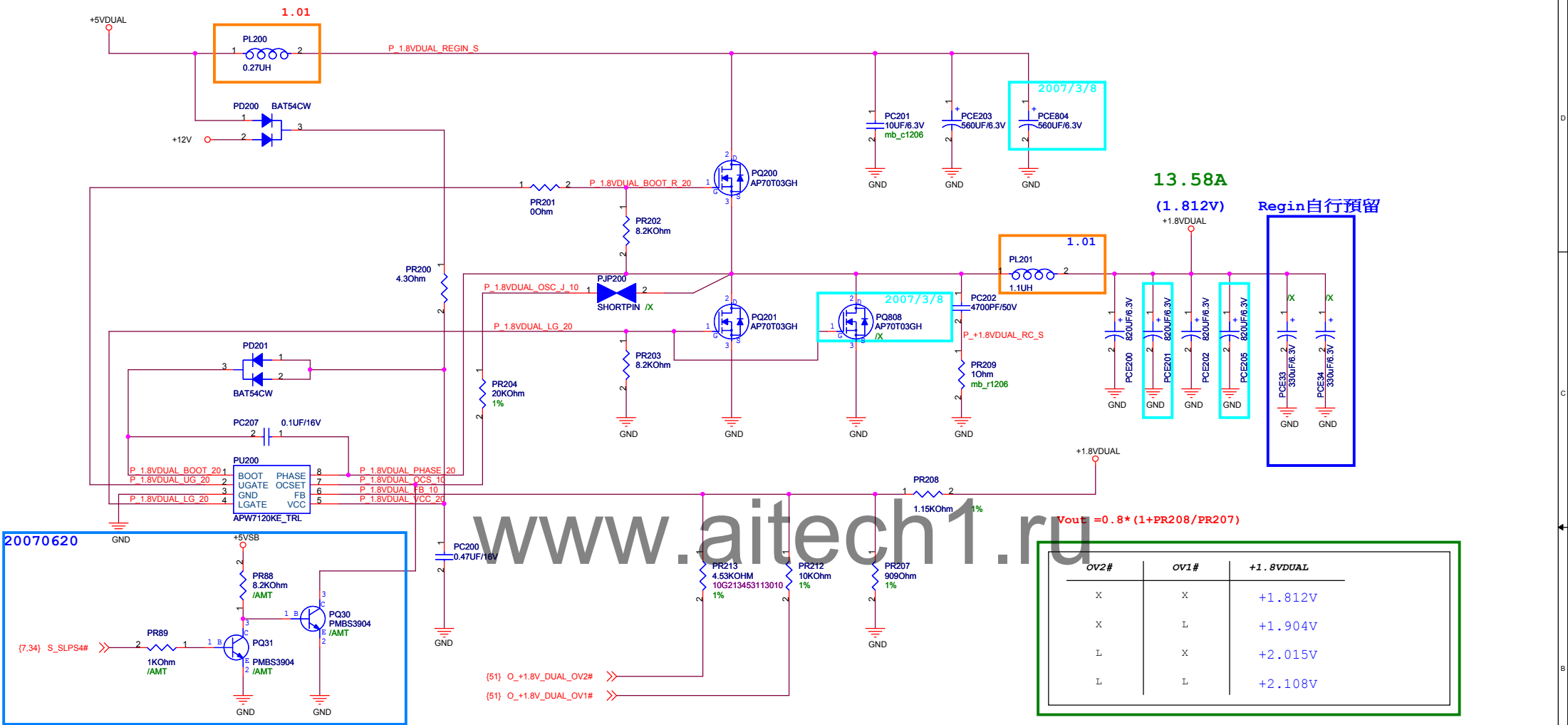


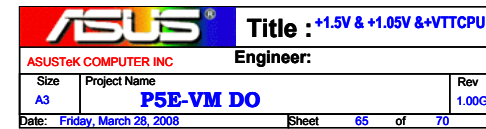
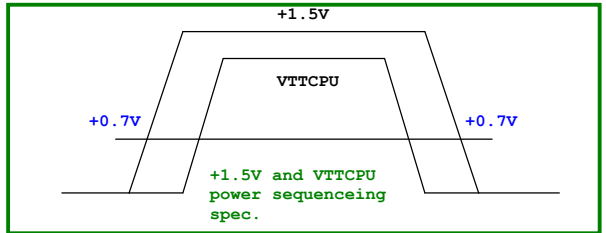
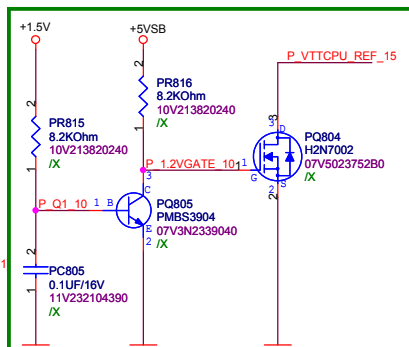
<Variant Name> +5V_DUAL&+3VSB&+3V_DUAL

2007/3/8

+5VDUAL_USBKB UVP CIRCUIT



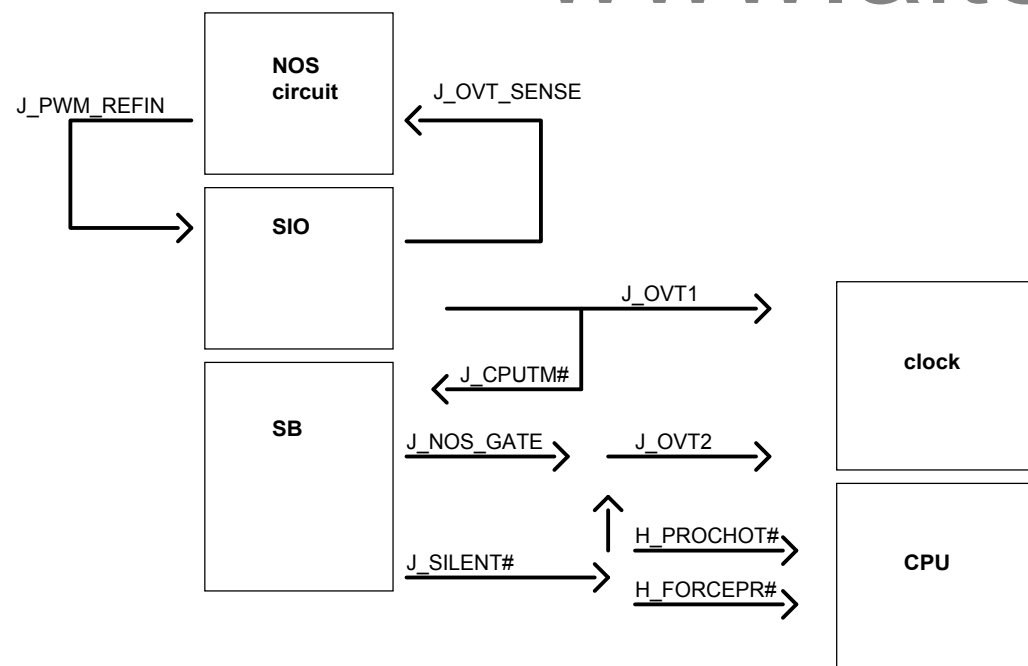




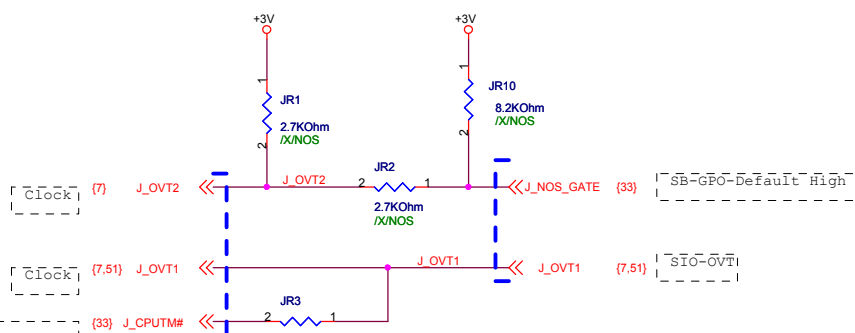
	J_OVT1	J_OVT2
NOS disable	Don't Care	1
NOS enable heavy loading	0	0
NOS enable normal loading	1	0

```
|SB-GPI |-----|
|BIOS can get OVT|
|state from this |
|pin.            |
|                |
```

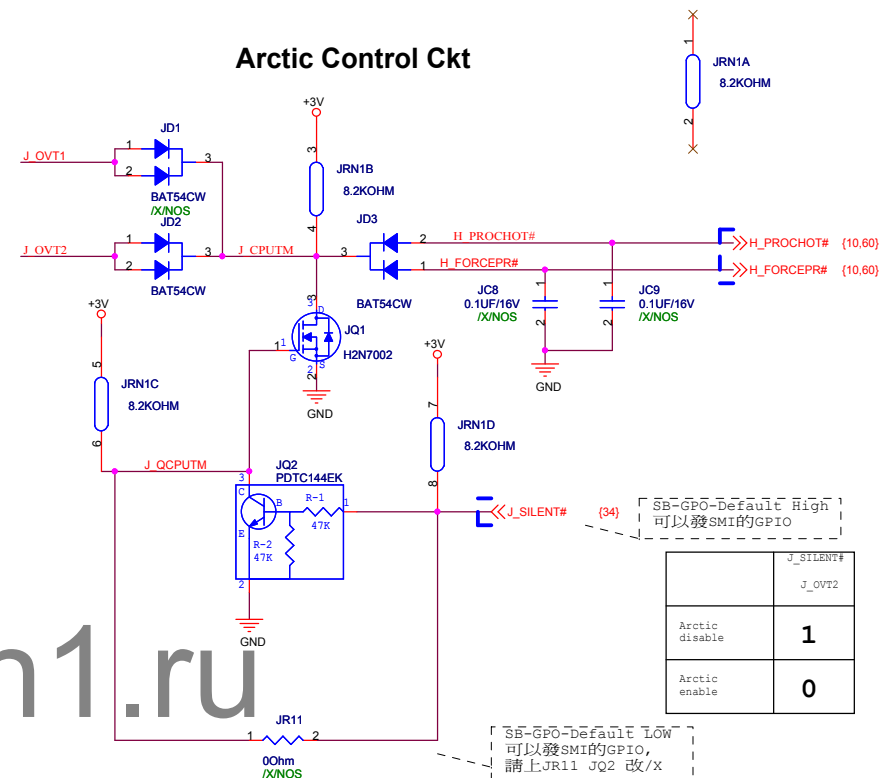
Function Block :



NOS Control Ckt



Arctic Control Ckt



	J_SILENT
	J_OVT2
Arctic disable	1
Arctic enable	0

	J_SILENT
	J_OVT2
Arctic disable	0
Arctic enable	1

Standard Circuit	
NOS	Intel
REV.	J_0.1B beta

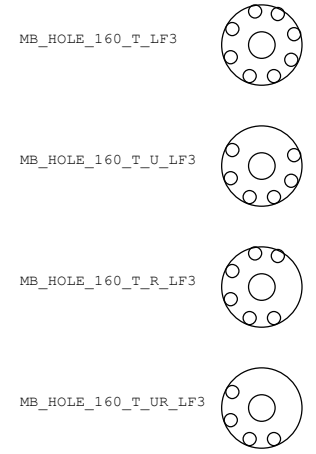
LOGO_STD_NOS
/X/NOS

<Variant Name>

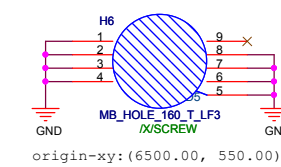
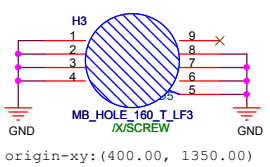
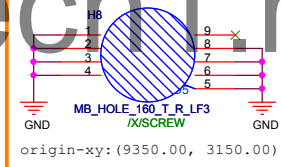
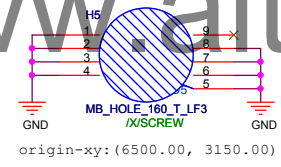
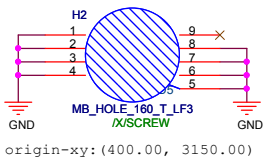
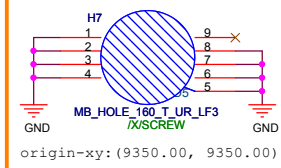
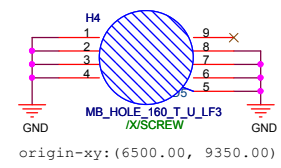
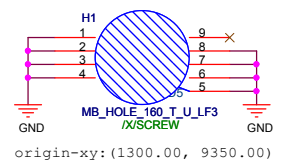
Screw Select

	Standard (9.6 x 9.6)	scale down (9.6 x <9.6)
H1	V	V
H2	V	V
H3	V	V
H4	V	V
H5	V	V
H6	V	V
H7	V	X
H8	V	X

MB SCREW FOOTPRINT



www.aitech1.ru



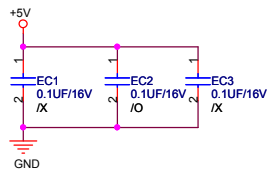
9.6 inch

(X,Y) = (0,0)

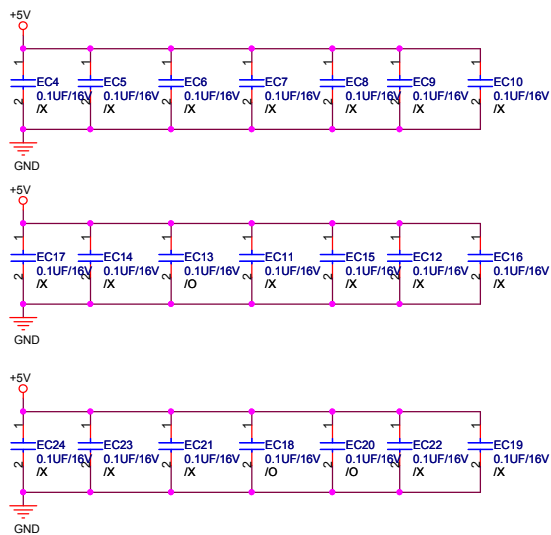
<9.6 inch

9.6 inch

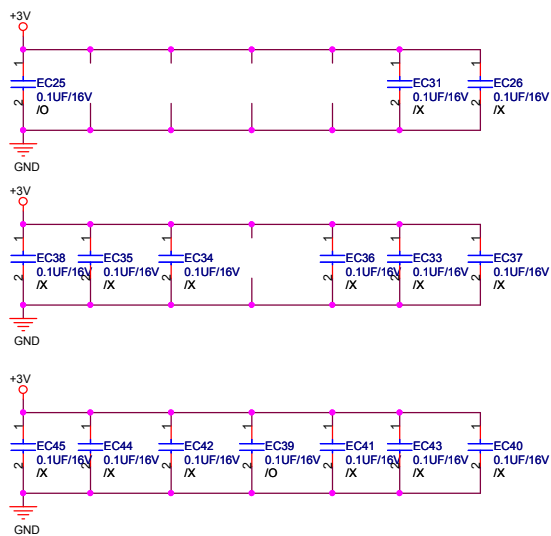
JMB368 FAE Suggestion
2007/03/13



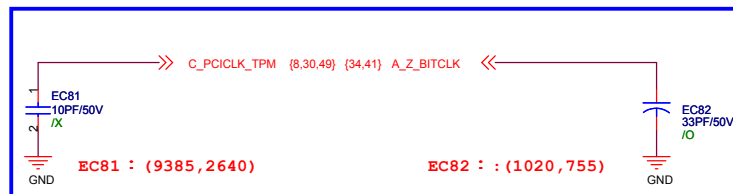
EC4-EC24 For EMI Used



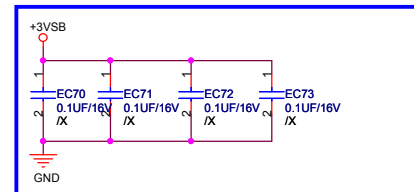
EC25-EC45 For EMI Used



2007/07/06

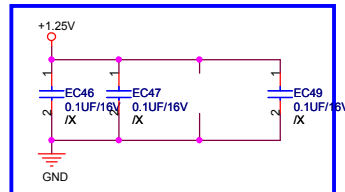


2007/07/05

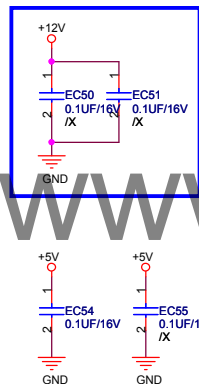


EC70 : (8365,9140)
EC71 : (9110,2890)
EC72 : (7240,925)
EC73 : (5470,1655)

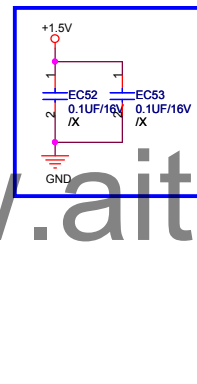
EC46-EC49 For EMI Used



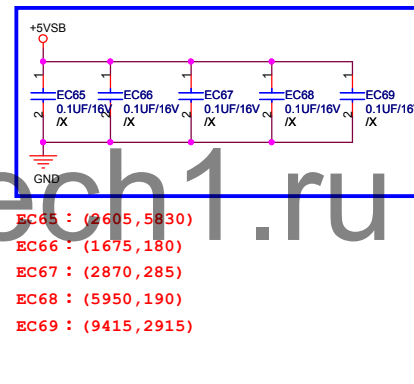
EC50-EC51 For EMI Used



EC52-EC53 For EMI Used

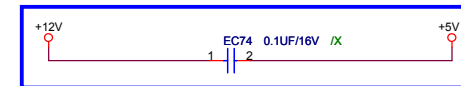


2007/07/05



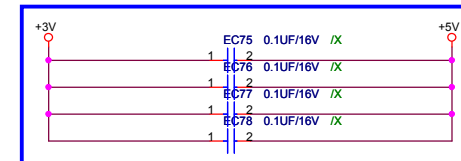
EC65 : (2605,5830)
EC66 : (1675,180)
EC67 : (2870,285)
EC68 : (5950,190)
EC69 : (9415,2915)

2007/07/05



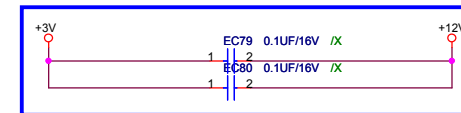
EC74 : (1370,3075)

2007/07/05



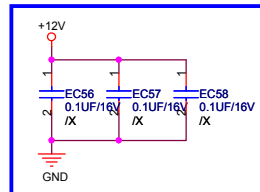
EC75 : (1740,3420)
EC76 : (3205,635)
EC77 : (4610,2145)
EC78 : (8120,835)

2007/07/05



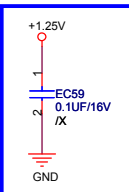
EC79 : (2020,2835)
EC80 : (8190,3760)

2007/07/05



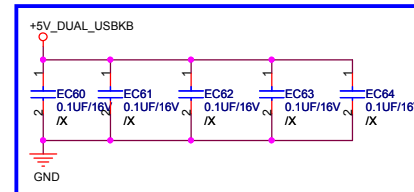
EC56 : (7075,2870)
EC57 : (4825,2200)
EC58 : (1140,6385)

2007/07/05



EC59 : (4300,3515)

2007/07/05



EC60 : (1370,5355)
EC61 : (1300,4755)
EC62 : (1855,425)
EC63 : (5855,465)
EC64 : (8505,420)

<Variant Name>

ASUS		Title : EMI CAP	
<OrgName>		Engineer: <OrgAddr1>	
Size A3	Project Name P5E-VM DO	Rev 1.00G	
Date: Friday, March 28, 2008		Sheet	69 of 70

PCB Rev	Change List
R1.00G	Initial Version
R1.01G	1. Swap SATA 3 & SATA 4 To support ICH9 Base version Chipset 2. Update Core team ASM4131 Standard circuit 3. Unify the Power Solution Choke for Channel request
R1.02G	1.Modify the SATA 3 port one set differential signals (Page 35) 2.Change VRN104 instead of VR40 & VR41 in order to reduce high speed differential signal stub effect (Page 24) 3.Add OR611 to reserve SIO PWROK issue to pull-up +3VSB(Page 53) 4. For All Channel Request to change Power Choke pitch size on PL102,PL103,PL104,PL201

www.aitech1.ru